

Compal Confidential

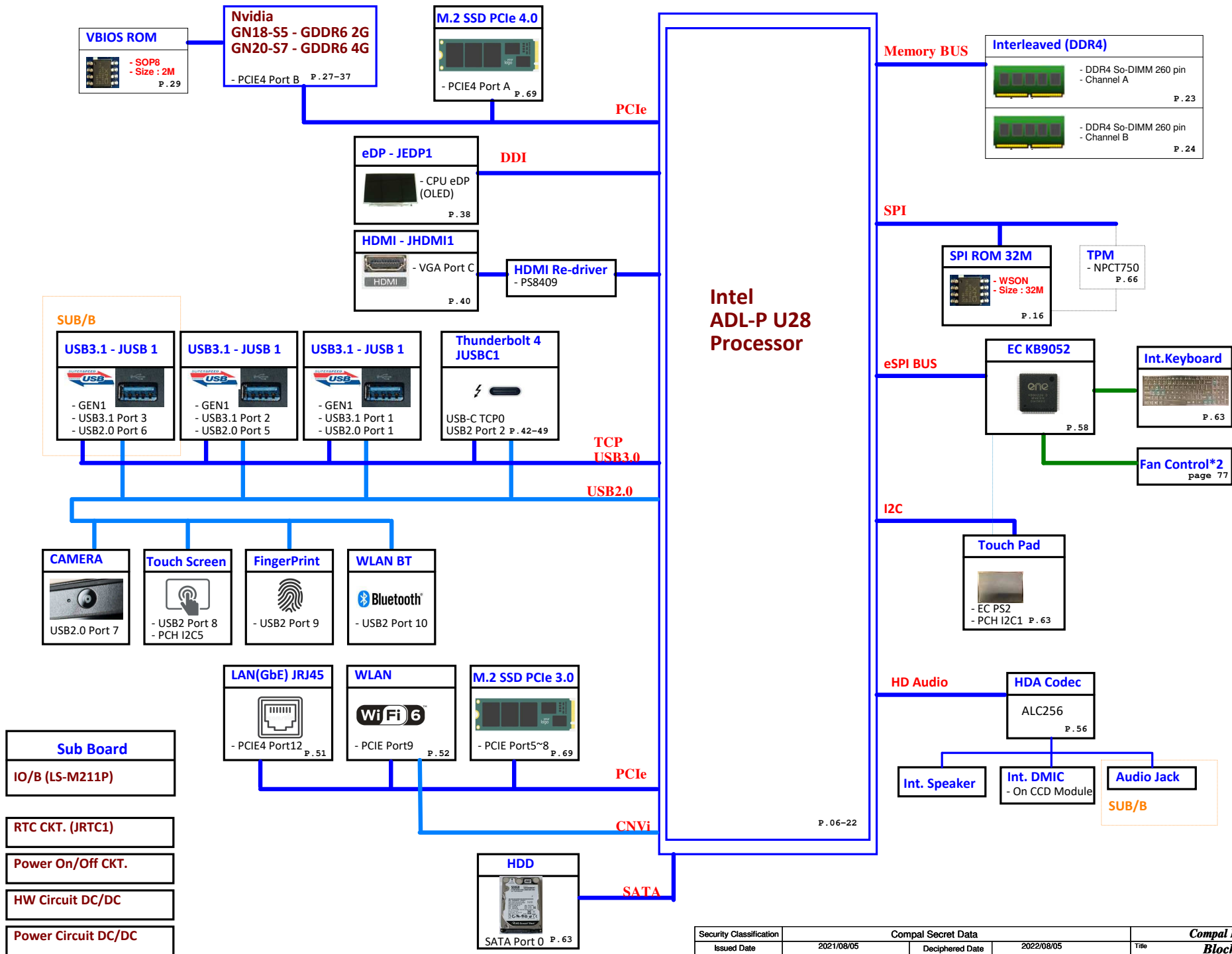
HH5A4 MB Schematic Document

LA-M211P

Rev : 1A

2022.04.18

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Issued Date	2021/08/05	Deciphered Date	2022/08/05	Title	Cover Sheet
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				HH5A4 MB LA-M211P	



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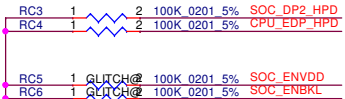
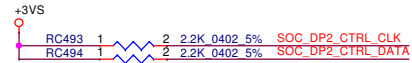
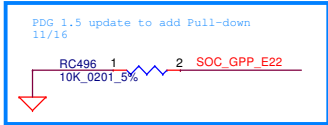
G3->S0

S0-> S0iX

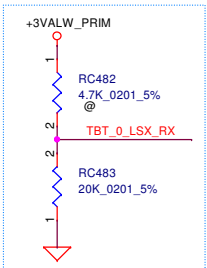
S0iX ->S0

S0->S5

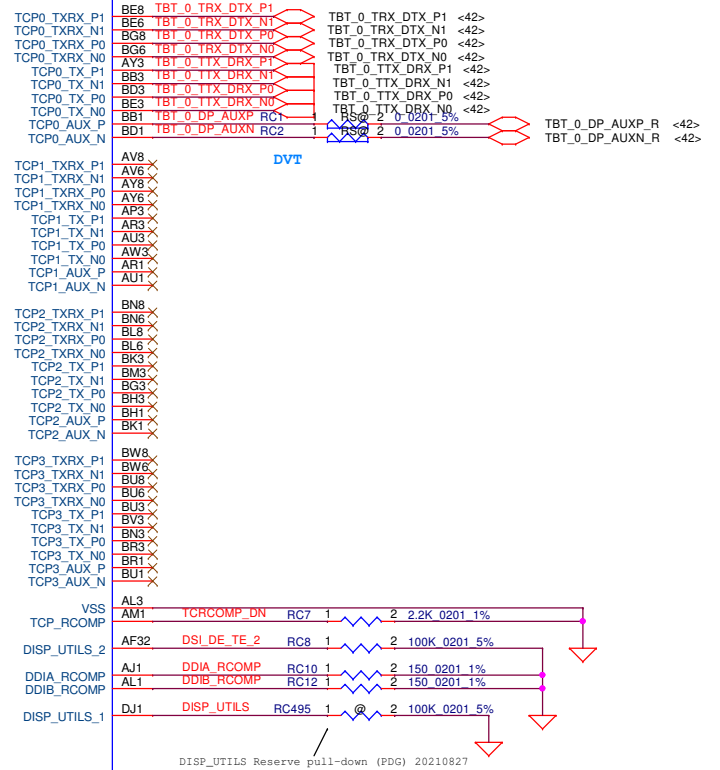
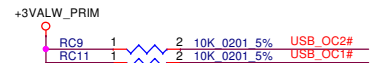




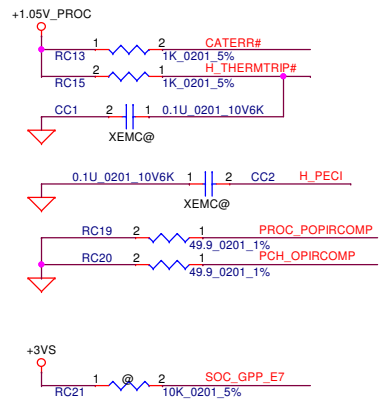
follow RVP



TBT_LSX #0 PINS VOCIO CONFIGURATION	
Weak Internal Pull down 20k	
SAMPLING - RSMRSTB	
HIGH	3.3V
LOW	1.8V



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CHECK power net name, 05/17

<58,85> H_PROCHOT#

check SW setting for leakage, 1225

<58,63> EC_TP_INT#

<56> PCH_SPKR

check SW setting, 1225

<17,43> VCCIN_AUX_CORE_ALERT#_R

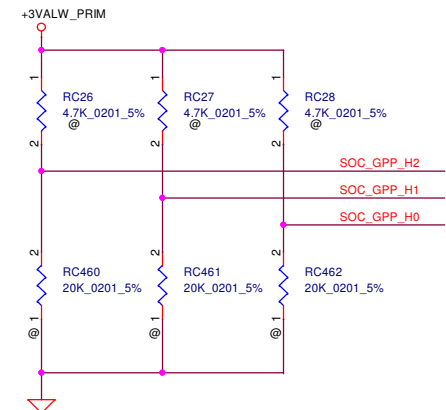
+1.05V_OUT_FET
RC23 1 CMC@ 2 1K_0201_5% XDP_ITP_PMODE

XDP_ITP_PMODE
DFX TEST MODE
INTERNAL PD 20K
This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Strap Pin



PCH_SPKR
SPKR
TOP SWAP OVERRIDE
INTERNAL PD 20K
HIGH: Top swap enable
LOW: Disable (Default)



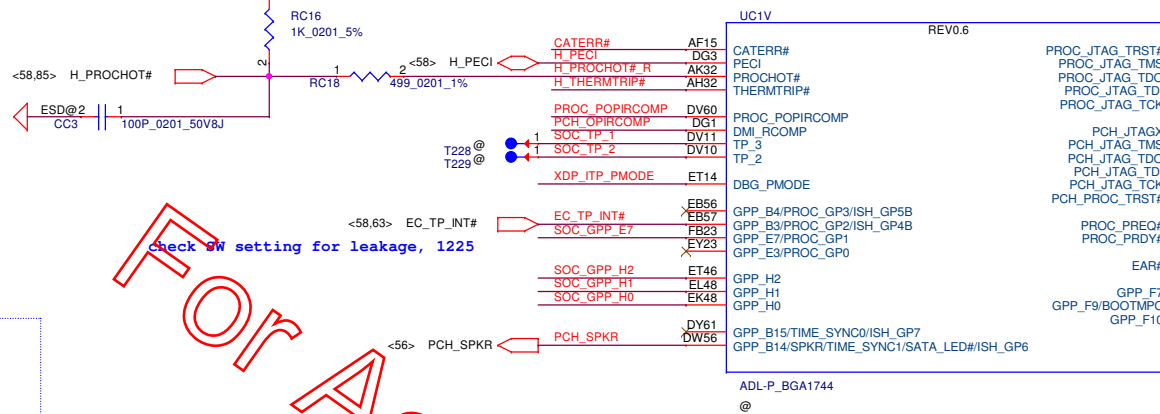
SOC_GPP_H0 GH4FT For RTD3 SSD
GH52T Remove 20200817

SOC_GPP_H2
BOOT STRAP3 - BIT3
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

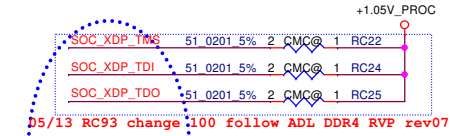
SOC_GPP_H1
BOOT STRAP1 - BIT2
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

SOC_GPP_H0
BOOT STRAP1 - BIT1
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

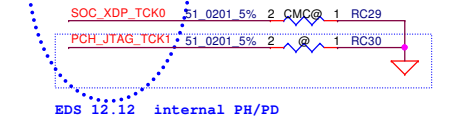
SOC_WWAN_RST# (No used)
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
INTERNAL PD 20K



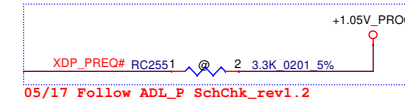
R6 SOC_XDP_TRST#
U8 SOC_XDP_TMS
AA6 SOC_XDP_TDO
W8 SOC_XDP_TDI
N6 SOC_XDP_TCK0
N8 SOC_XDP_TCK0
U6 SOC_XDP_TMS
AA8 SOC_XDP_TDO
W6 SOC_XDP_TDI
FB6 PCH_JTAG_TCK1
R8 SOC_XDP_TRST#
L6 XDP_PREQ#
L8 XDP_PRDY#
AF25 SOC_EAR#
EN28
ET28
EF28
GPP_F7
GPP_F9/BOOTMPC
GPP_F10



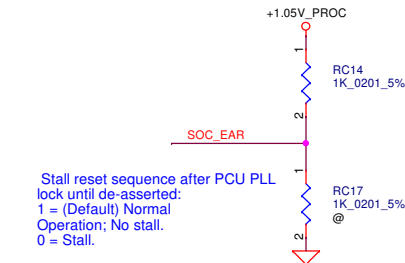
D5/13 RC93 change 100 follow ADL DDR4 RVP rev07



EDS 12.12 internal PH/PD



05/17 Follow ADL_P SchChk_rev1.2

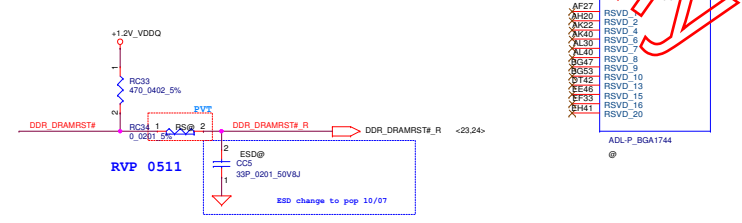
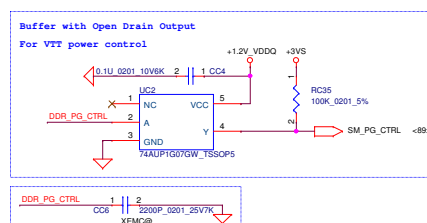


Stall reset sequence after PCU PLL lock until de-asserted:
1 = (Default) Normal Operation; No stall.
0 = Stall.

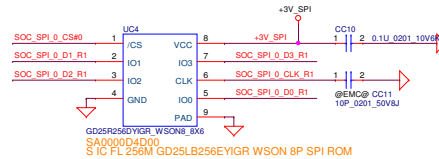
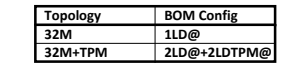
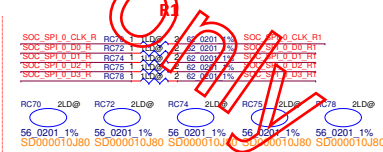
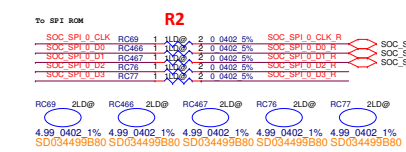
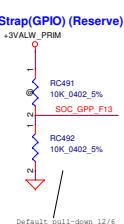
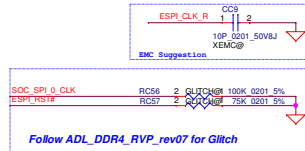
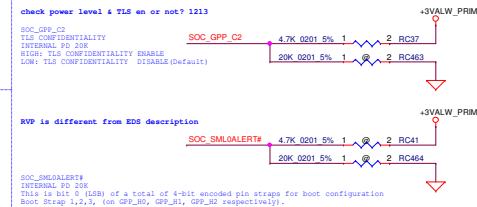
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Issued Date	2021/08/05	Deciphered Date	2022/08/05	Title	ADL-P(2/14)MISC,XDP
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Follow Intel DDR4 N1L

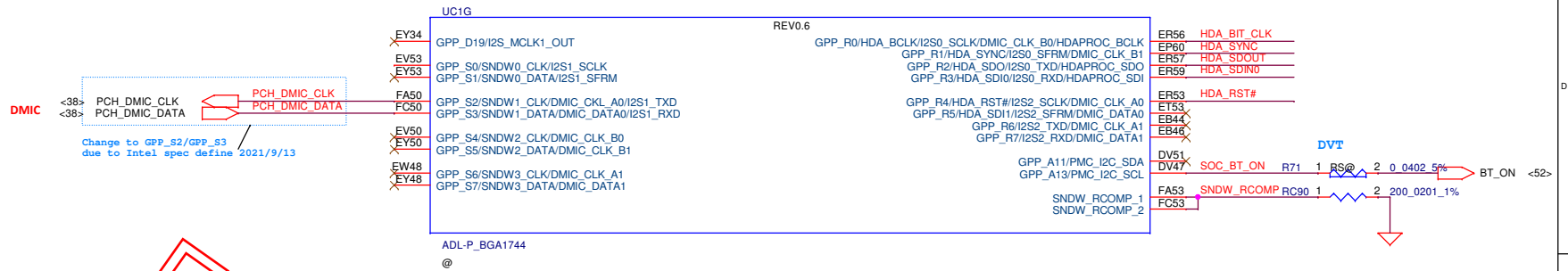
DDR4: Refer to ADL_P_DDR4_SODIMM_1DPC_RVP_Rev0p7



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				HHS54 MB LA-M21P1	Rev 1A
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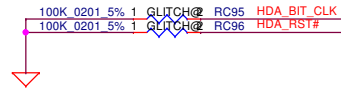
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Issued Date	2021/08/05	Deciphered Date	2022/08/05	Title	
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Date:	2023-Apr-18 10:29	Sheet	9	of	150



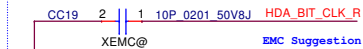
HDA for AUDIO

20200819
- Remove RC180 BOM config., must pop of PDG.

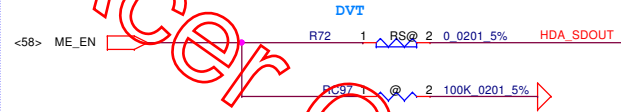
<56>	HDA_SDOUT_R	HDA_SDOUT_R	RC31	1	2	33	0201	5%	HDA_SDOUT
<56>	HDA_BIT_CLK_R	HDA_BIT_CLK_R	RC32	1	2	33	0201	5%	HDA_BIT_CLK
<56>	HDA_SYNC_R	HDA_SYNC_R	RC93	1	2	33	0201	5%	HDA_SYNC
<56>	HDA_RST#_R	HDA_RST#_R	RC94	1	2	33	0201	5%	HDA_RST#
<56>	HDA_SDI0	HDA_SDI0							



Follow
627205_ADL_P_PDG for Glitch



To Enable ME Override



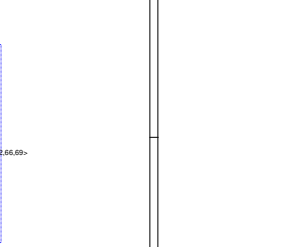
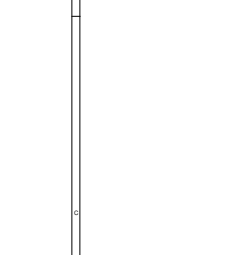
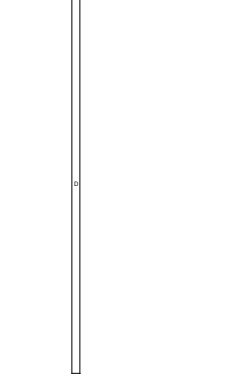
572631_ICL_PCH_LP_EDS_Vol_1_Rev_0p9
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO

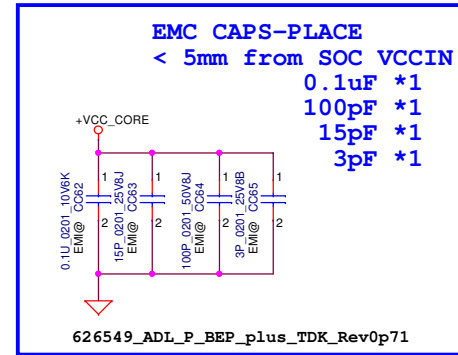
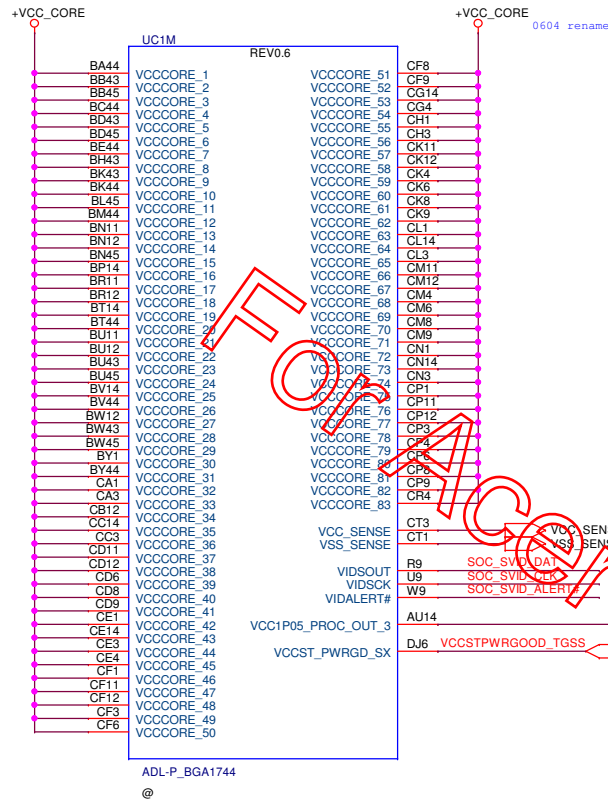
HDA_SDOUT
FLASH_DESCRIPTOR SECURITY OVERRIDE
INTERNAL PD 20K
HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN (DEFAULT)

HDA_SYNC	CC12	@RF@1	2	22P	0201	25V8
HDA_BIT_CLK	CC13	@RF@1	2	22P	0201	25V8
HDA_SDOUT	CC14	@RF@1	2	22P	0201	25V8
HDA_SDI0	CC15	@RF@1	2	22P	0201	25V8
HDA_RST#	CC16	@RF@1	2	22P	0201	25V8
PCH_DMIC_CLK	CC17	@RF@1	2	22P	0201	25V8
PCH_DMIC_DATA	CC18	@RF@1	2	22P	0201	25V8

Close SOC

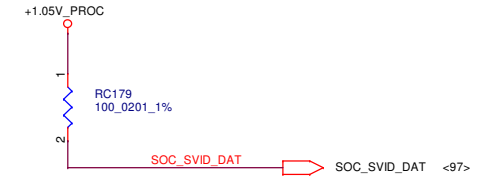
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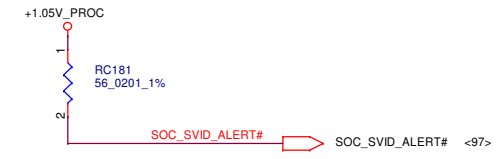


Stitching Cap.

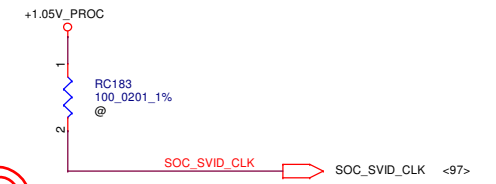
SVID DATA



SVID ALERT



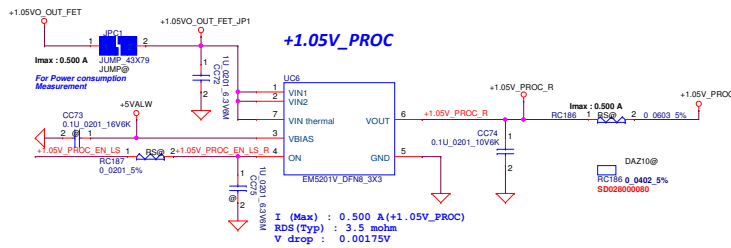
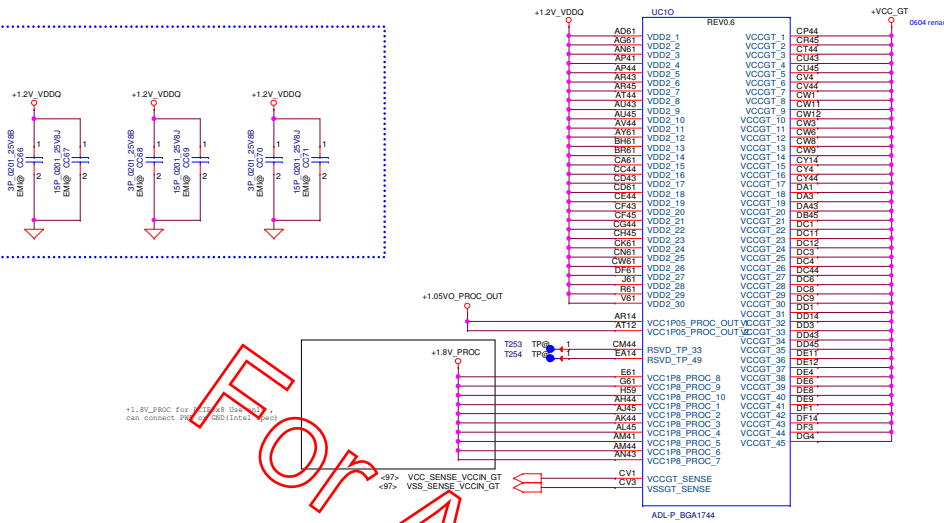
SVID CLOCK



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EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
15pF* 3 (EMI@)
3pF* 3 (EMI@)

627333_ADL_P_DDR4_RVP_TDK_Rev0p7

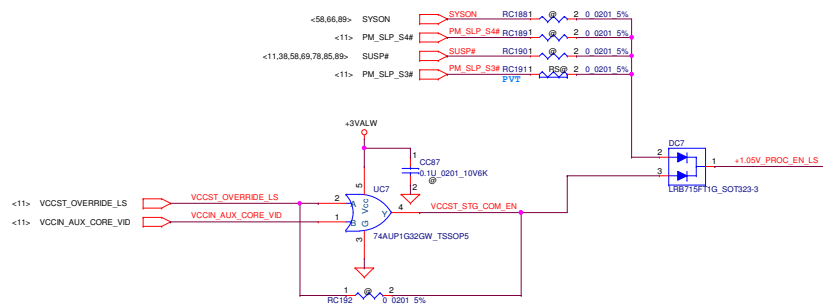


627205_ADL_P_PD6_Rev1.2

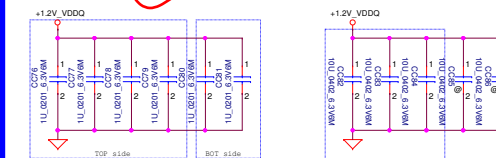
NOTE

Sideband signals(PECI,THERMTRIP,PROCHOT,VCCST_PWRGD,SVID) should be connected to **VCC1P05_PROC** rail when there is Power Gate or to **VCC1P05_OUT_FET** (which should be shorted to VCC1P05_OUT_FET) rail when there is no Power Gate.

+1.05V_PROC Enable



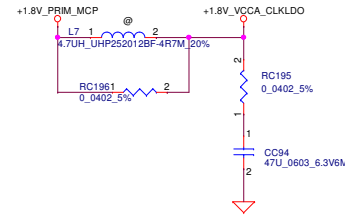
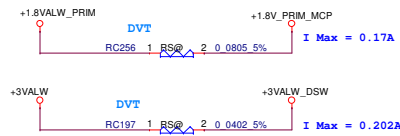
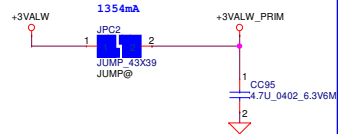
1uF* 3
10uF* 3
1uF* 3
Layout Follow 627205_ADL_P_PD6_Rev0p7



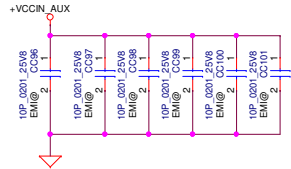
+1.8V_PROC for PCIe5d Use only ,
can connect PWB or GND(Intel spec) 10/8

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+3VALW TO +3V_PRIM



EMC CAPS-PLACE < 5mm from SOC VCCIN_AUX



For CS Use Only

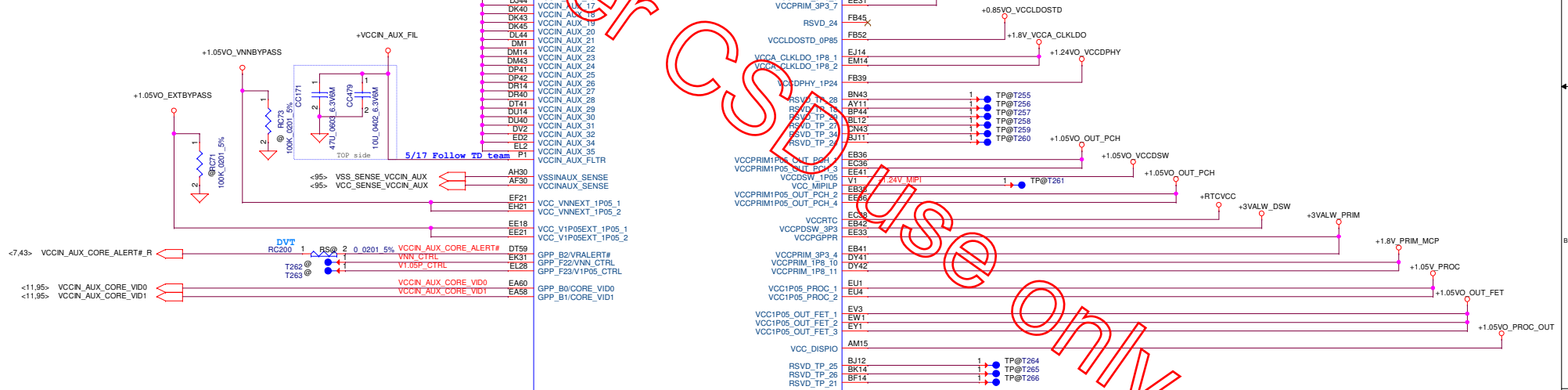
Note: VCCPGPPR follow HDA interface 11.2.2.6 VCCPGPPR

Description: Intel HD Audio Supply. Can operate at 3.3V or 1.8V

Settings

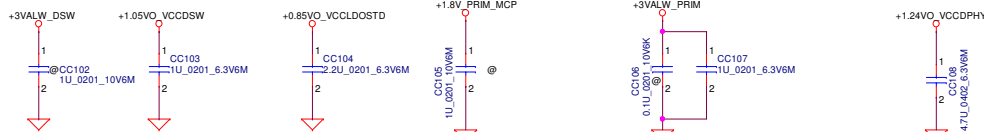
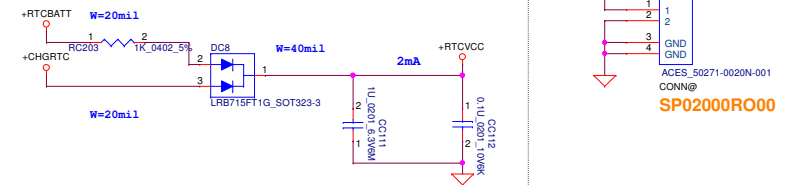
Table 818. Reference Layout Design

Index	Design Note	Reference Design
1	VCCPGPPR can be merged directly to either VCCPRIM_3P3 or VCCPRIM_1P8 power plane depending on the operating voltage. Required immediate ground reference for VCCPGPPR power plane.	GPPR_1
2	If operating at 3.3V: Merge VCCPGPPR PTH with VCCPRIM_3P3 plane.	GPPR_1
3	If operating at 1.8V: Extend VCCPGPPR to merge with VCCPRIM_1P8 plane.	GPPR_2



RTC Battery

MAX. 8000mili



PLACE CAP CLOSEST POSSIBLE TO THE BGA

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		Size	Document Number
		HHS44 MB LA-M211P	
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UC1P		
REV0.6		
A3	VSS_7	VSS_74
A10	VSS_1	VSS_75
A21	VSS_2	VSS_76
A23	VSS_3	VSS_77
A25	VSS_4	VSS_78
A26	VSS_5	VSS_79
A28	VSS_6	VSS_80
A30	VSS_8	VSS_81
A31	VSS_9	VSS_82
A33	VSS_10	VSS_83
A40	VSS_11	VSS_84
A47	VSS_12	VSS_85
A53	VSS_13	VSS_86
A60	VSS_14	VSS_87
AA11	VSS_15	VSS_88
AA21	VSS_16	VSS_89
AA26	VSS_17	VSS_90
AA31	VSS_18	VSS_91
AA35	VSS_19	VSS_92
AA40	VSS_20	VSS_93
AA44	VSS_21	VSS_94
AA57	VSS_22	VSS_95
AA59	VSS_23	VSS_96
AB16	VSS_24	VSS_97
AB21	VSS_25	VSS_98
AB26	VSS_26	VSS_99
AB31	VSS_27	VSS_100
AB35	VSS_28	VSS_101
AB54	VSS_29	VSS_102
AC4	VSS_30	VSS_103
AC40	VSS_31	VSS_104
AC44	VSS_32	VSS_105
AC51	VSS_33	VSS_106
AC55	VSS_34	VSS_107
AC6	VSS_35	VSS_108
AC8	VSS_36	VSS_109
AD21	VSS_37	VSS_110
AD26	VSS_38	VSS_111
AD31	VSS_39	VSS_112
AD35	VSS_40	VSS_113
AD46	VSS_41	VSS_114
AD48	VSS_42	VSS_115
AD58	VSS_43	VSS_116
AE12	VSS_44	VSS_117
AE17	VSS_45	VSS_118
AE22	VSS_46	VSS_119
AE27	VSS_47	VSS_120
AE32	VSS_48	VSS_121
AE37	VSS_49	VSS_122
AE40	VSS_50	VSS_123
AE44	VSS_51	VSS_124
AE52	VSS_52	VSS_125
AE9	VSS_53	VSS_126
AF4	VSS_54	VSS_127
AF46	VSS_55	VSS_128
AG1	VSS_56	VSS_129
AG51	VSS_57	VSS_130
AG55	VSS_58	VSS_131
AG58	VSS_59	VSS_132
AH9	VSS_60	VSS_133
AJ3	VSS_61	VSS_134
AJ41	VSS_62	VSS_135
AJ47	VSS_63	VSS_136
AJ49	VSS_64	VSS_137
AJ54	VSS_65	VSS_138
AK20	VSS_66	VSS_139
AK25	VSS_67	VSS_140
AK30	VSS_68	VSS_141
AK37	VSS_69	VSS_142
AK4	VSS_70	VSS_143
AK57	VSS_71	VSS_144
AK59	VSS_72	VSS_145
AK9	VSS_73	VSS_146

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UC1Q		
REV0.6		
BF58	VSS_149	VSS_222
BG1	VSS_150	VSS_223
BG12	VSS_151	VSS_224
BG44	VSS_152	VSS_225
BG52	VSS_153	VSS_226
BG9	VSS_154	VSS_227
BH4	VSS_155	VSS_228
BH46	VSS_156	VSS_229
BH48	VSS_157	VSS_230
BH58	VSS_158	VSS_231
BJ51	VSS_159	VSS_232
BJ55	VSS_160	VSS_233
BJ6	VSS_161	VSS_234
BJ8	VSS_162	VSS_235
BJ9	VSS_163	VSS_236
BL11	VSS_164	VSS_237
BL4	VSS_165	VSS_238
BL54	VSS_166	VSS_239
BL9	VSS_167	VSS_240
BM1	VSS_168	VSS_241
BM14	VSS_169	VSS_242
BM47	VSS_170	VSS_243
BM59	VSS_171	VSS_244
BN1	VSS_172	VSS_245
BN54	VSS_173	VSS_246
BN9	VSS_174	VSS_247
BP4	VSS_175	VSS_248
BP51	VSS_176	VSS_249
BP55	VSS_177	VSS_250
BR43	VSS_178	VSS_251
BR46	VSS_179	VSS_252
BR48	VSS_180	VSS_253
BR48	VSS_181	VSS_254
BR58	VSS_182	VSS_255
BR6	VSS_183	VSS_256
BR8	VSS_184	VSS_257
BR9	VSS_185	VSS_258
BT4	VSS_186	VSS_259
BT51	VSS_187	VSS_260
BT55	VSS_188	VSS_261
BU54	VSS_189	VSS_262
BU9	VSS_190	VSS_263
BV1	VSS_191	VSS_264
BV47	VSS_192	VSS_265
BV57	VSS_193	VSS_266
BV59	VSS_194	VSS_267
BW4	VSS_195	VSS_268
BW54	VSS_196	VSS_269
BW9	VSS_197	VSS_270
BY3	VSS_198	VSS_271
C1	VSS_199	VSS_272
C21	VSS_200	VSS_273
C25	VSS_201	VSS_274
C28	VSS_202	VSS_275
C31	VSS_203	VSS_276
C34	VSS_204	VSS_277
C40	VSS_205	VSS_278
C47	VSS_206	VSS_279
C9	VSS_207	VSS_280
CA14	VSS_208	VSS_281
CA43	VSS_209	VSS_282
CA46	VSS_210	VSS_283
CA48	VSS_211	VSS_284
CA51	VSS_212	VSS_285
CA55	VSS_213	VSS_286
CA58	VSS_214	VSS_287
CB4	VSS_215	VSS_288
CB6	VSS_216	VSS_289
CB8	VSS_217	VSS_290
CB9	VSS_218	VSS_291
CC1	VSS_219	VSS_292
CC52	VSS_220	VSS_293
CD46	VSS_221	VSS_294

ADL-P_BGA1744

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UC1R		
REV0.6		
DC47	VSS_295	VSS_369
DC54	VSS_296	VSS_370
DC57	VSS_297	VSS_371
DC59	VSS_298	VSS_372
DE44	VSS_299	VSS_373
DE51	VSS_300	VSS_374
DE55	VSS_301	VSS_375
DF43	VSS_302	VSS_376
DF46	VSS_303	VSS_377
DF48	VSS_304	VSS_378
DF58	VSS_305	VSS_379
DG11	VSS_306	VSS_380
DG12	VSS_307	VSS_381
DG51	VSS_308	VSS_382
DG55	VSS_309	VSS_383
DG59	VSS_310	VSS_384
DG8	VSS_311	VSS_385
DG9	VSS_312	VSS_386
DH4	VSS_313	VSS_387
DH54	VSS_314	VSS_388
DJ47	VSS_315	VSS_389
DJ57	VSS_316	VSS_390
DJ59	VSS_317	VSS_391
DK14	VSS_318	VSS_392
DK54	VSS_319	VSS_393
DL10	VSS_320	VSS_394
DL11	VSS_321	VSS_395
DL13	VSS_322	VSS_396
DM4	VSS_323	VSS_397
DM41	VSS_324	VSS_398
DM45	VSS_325	VSS_399
DM48	VSS_326	VSS_400
DM51	VSS_327	VSS_401
DM55	VSS_328	VSS_402
DM58	VSS_329	VSS_403
DM61	VSS_330	VSS_404
DN13	VSS_331	VSS_405
DN40	VSS_332	VSS_406
DN8	VSS_333	VSS_407
DP46	VSS_334	VSS_408
DP49	VSS_335	VSS_409
DT13	VSS_336	VSS_410
DT52	VSS_337	VSS_411
DT8	VSS_338	VSS_412
DV13	VSS_339	VSS_413
DV4	VSS_340	VSS_414
DV41	VSS_341	VSS_415
DV43	VSS_342	VSS_416
DV46	VSS_343	VSS_417
DV51	VSS_344	VSS_418
DV55	VSS_345	VSS_419
DV6	VSS_346	VSS_420
DV8	VSS_347	VSS_421
DW14	VSS_348	VSS_422
DW25	VSS_349	VSS_423
DW35	VSS_350	VSS_424
DY13	VSS_351	VSS_425
DY33	VSS_352	VSS_426
DY36	VSS_353	VSS_427
DY38	VSS_354	VSS_428
DY62	VSS_355	VSS_429
DY8	VSS_356	VSS_430
E43	VSS_357	VSS_431
E50	VSS_358	VSS_432
EB13	VSS_359	VSS_433
EB25	VSS_360	VSS_434
EB26	VSS_361	VSS_435
EB31	VSS_362	VSS_436
EC11	VSS_363	VSS_437
EC21	VSS_364	VSS_438
EC28	VSS_365	VSS_439
ED13	VSS_366	VSS_440
ED4	VSS_367	VSS_441
ED56	VSS_368	VSS_442

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UC1S		
REV0.6		
F56	VSS_443	VSS_517
F59	VSS_444	VSS_518
F9	VSS_445	VSS_519
FA40	VSS_446	VSS_520
FA7	VSS_447	VSS_521
FB1	VSS_448	VSS_522
FB14	VSS_449	VSS_523
FB26	VSS_450	VSS_524
FB42	VSS_451	VSS_525
FB48	VSS_452	VSS_526
FB59	VSS_453	VSS_527
FB61	VSS_454	VSS_528
FC2	VSS_455	VSS_529
FC55	VSS_456	VSS_530
FC56	VSS_457	VSS_531
FC58	VSS_458	VSS_532
FC60	VSS_459	VSS_533
G21	VSS_460	VSS_534
G25	VSS_461	VSS_535
G28	VSS_462	VSS_536
G31	VSS_463	VSS_537
G34	VSS_464	VSS_538
G42	VSS_465	VSS_539
G43	VSS_466	VSS_540
G50	VSS_467	VSS_541
H1	VSS_468	VSS_542
H13	VSS_469	VSS_543
H16	VSS_470	VSS_544
H18	VSS_471	VSS_545
H34	VSS_472	VSS_546
H37	VSS_473	VSS_547
H52	VSS_474	VSS_548
H58	VSS_475	VSS_549
H6	VSS_476	VSS_550
H8	VSS_477	VSS_551
H9	VSS_478	VSS_552
J11	VSS_479	VSS_553
J14	VSS_480	VSS_554
J17	VSS_481	VSS_555
J20	VSS_482	VSS_556
J21	VSS_483	VSS_557
J25	VSS_484	VSS_558
J28	VSS_485	VSS_559
J31	VSS_486	VSS_560
J36	VSS_487	VSS_561
J39	VSS_488	VSS_562
J47	VSS_489	VSS_563
J48	VSS_490	VSS_564
J51	VSS_491	VSS_565
J55	VSS_492	VSS_566
K4	VSS_493	VSS_567
L12	VSS_494	VSS_568
L13	VSS_495	VSS_569
L15	VSS_496	VSS_570
L17	VSS_497	VSS_571
L18	VSS_498	VSS_572
L20	VSS_499	VSS_573
L22	VSS_500	VSS_574
L23	VSS_501	VSS_575
L27	VSS_502	VSS_576
L30	VSS_503	VSS_577
L33	VSS_504	VSS_578
L35	VSS_505	VSS_579
L36	VSS_506	VSS_580
L38	VSS_507	VSS_581
L40	VSS_508	VSS_582
L54	VSS_509	VSS_583
L9	VSS_510	VSS_584
M16	VSS_511	VSS_585
M21	VSS_512	VSS_586
M26	VSS_513	VSS_587
M31	VSS_514	VSS_588
M34	VSS_515	VSS_589
M36	VSS_516	VSS_590

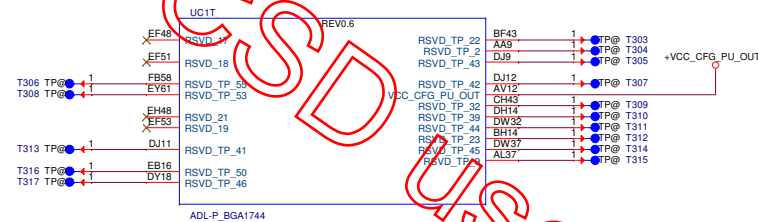
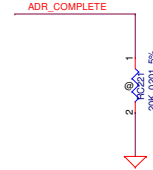
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T267 TP@

follow RVP

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				ADL-P(13/14)GND					
				Size		Document Number		Rev	
				HH5A4 MB LA-M211P		1A			
				Date:		Monday, April 18, 2022			
				Sheet		18 of 122			



Signal: CFG4 (Ref : MoW WW37)
The CFG [4] pin is made Reserved. Pull -Down termination recommendation is added wherever applicable.

For Acer CSD use only

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					Rev
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					Sheet 20 of 122
					1A
					HH5A4 MB LA-M211P

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			HH5A4 MB LA-M211P		1A
		Date:	Monday, April 18, 2022	Sheet	21

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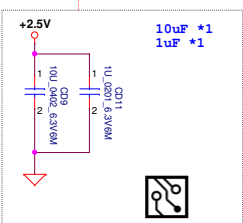
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2021/08/05	Deciphered Date	2022/08/05	Title	
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		Size			Document Number	Rev
		Date:			Monday, April 18, 2022	Sheet 22 of 122
		3	2	1	1A	

CHANNEL-A (Interleaved Memory)
> BOT : Reverse type (4mm)
> Non-ECC SO-DIMM

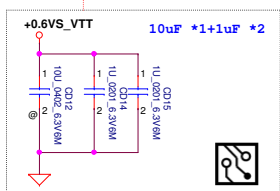
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Decoupling Cap._Channel A

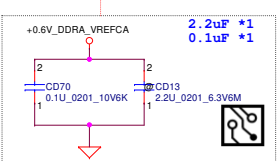
Layout Note:
Place near JDIMM1B.257,259



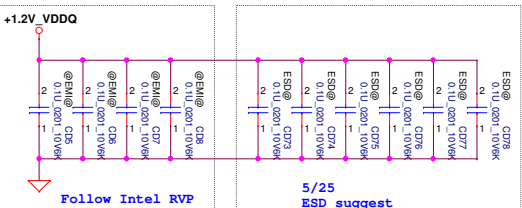
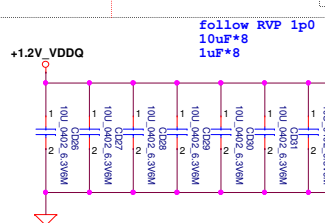
Layout Note:
Place near JDIMM1B.258



Layout Note:
PLACE THE CAP near JDIMM1B. 164

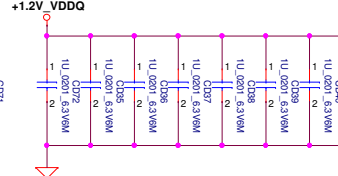


Layout Note:
Place near JDIMM2

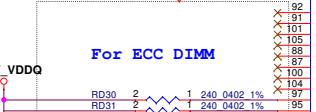
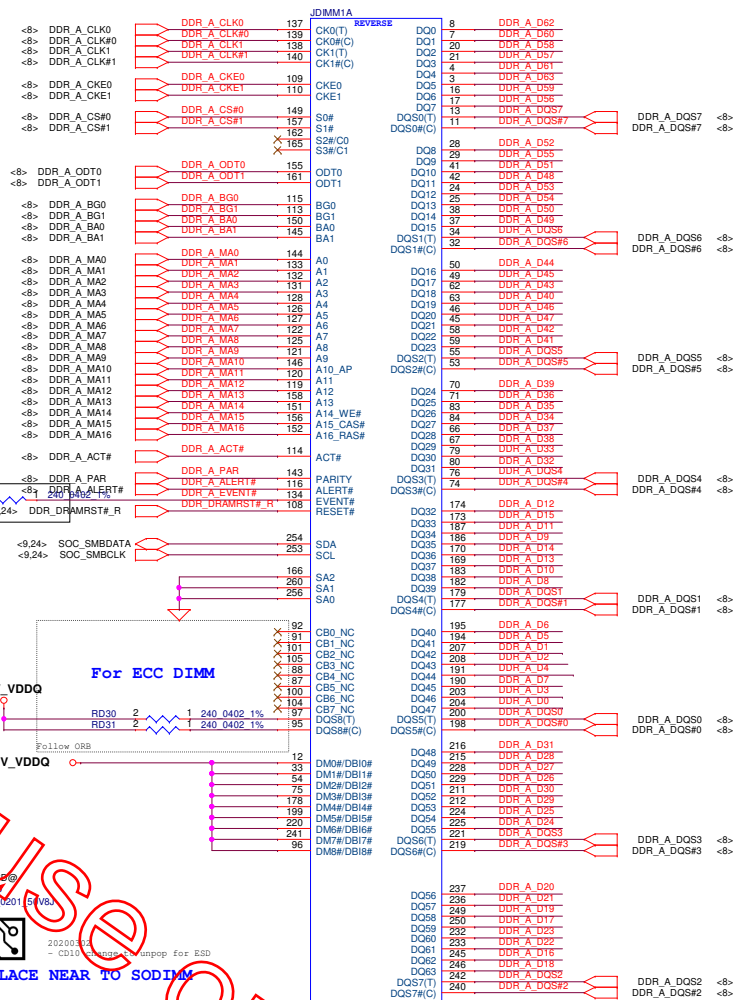


Follow Intel RVP

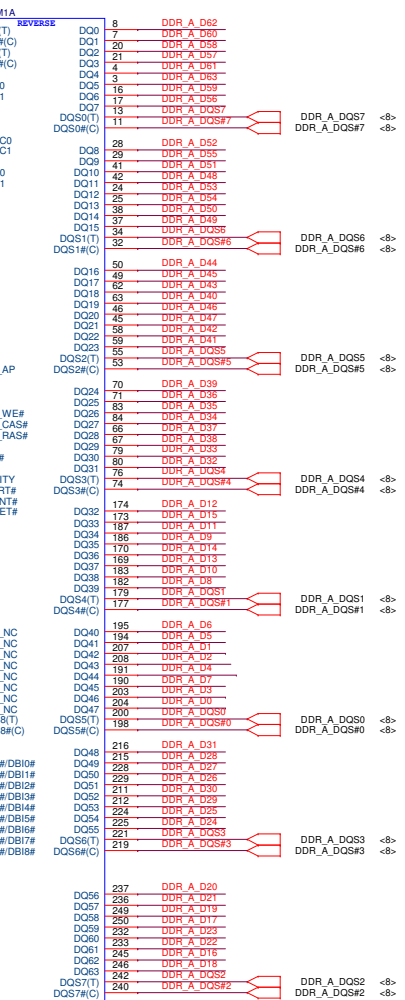
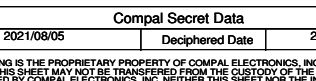
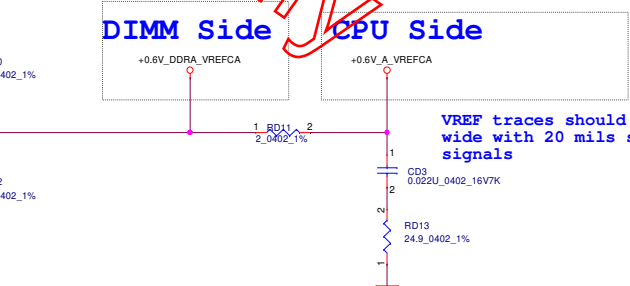
5/25 ESD suggest



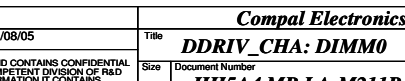
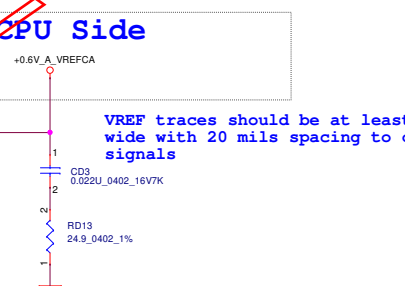
Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD



1 Max = 3.44A
2 channel --> 3.44 / 2 = 1.72A



1 Max = 3.44A
2 channel --> 3.44 / 2 = 1.72A



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CHANNEL-B (Interleaved Memory)

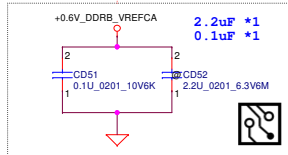
> BOT : STD type (4mm)

> Non-ECC SO-DIMM

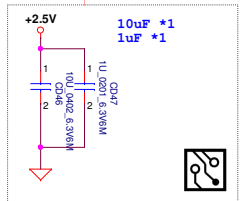
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 3200 MT/S

Decoupling Cap_Channel B

Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1

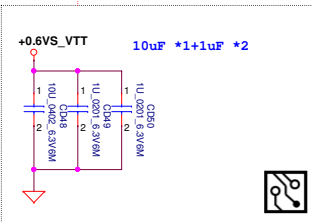


Layout Note:
Place near JDIMM2B.257,259

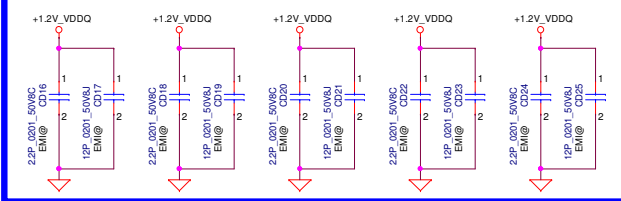


Layout Note:
Place near JDIMM2

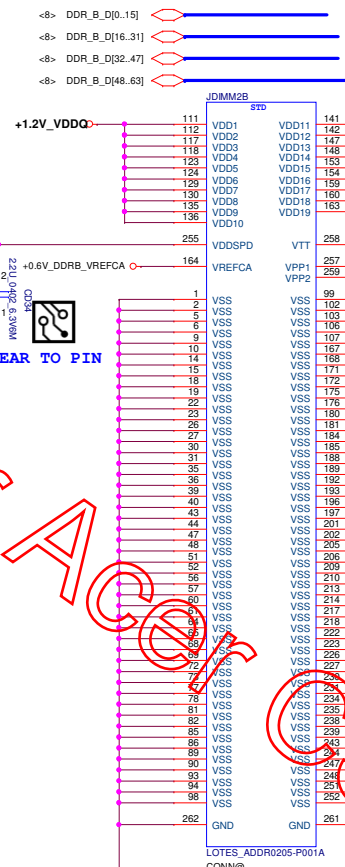
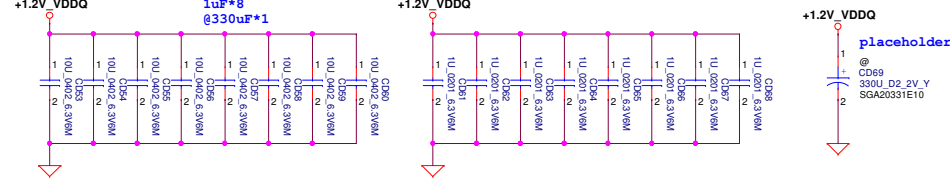
Layout Note:
Place near JDIMM2B.258



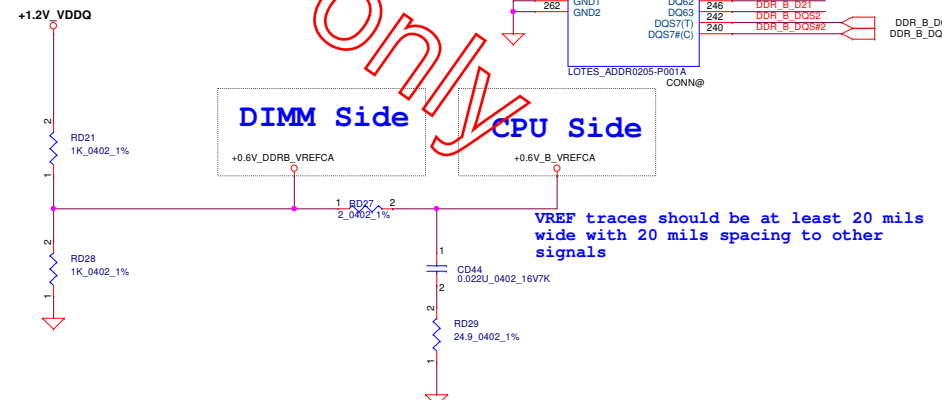
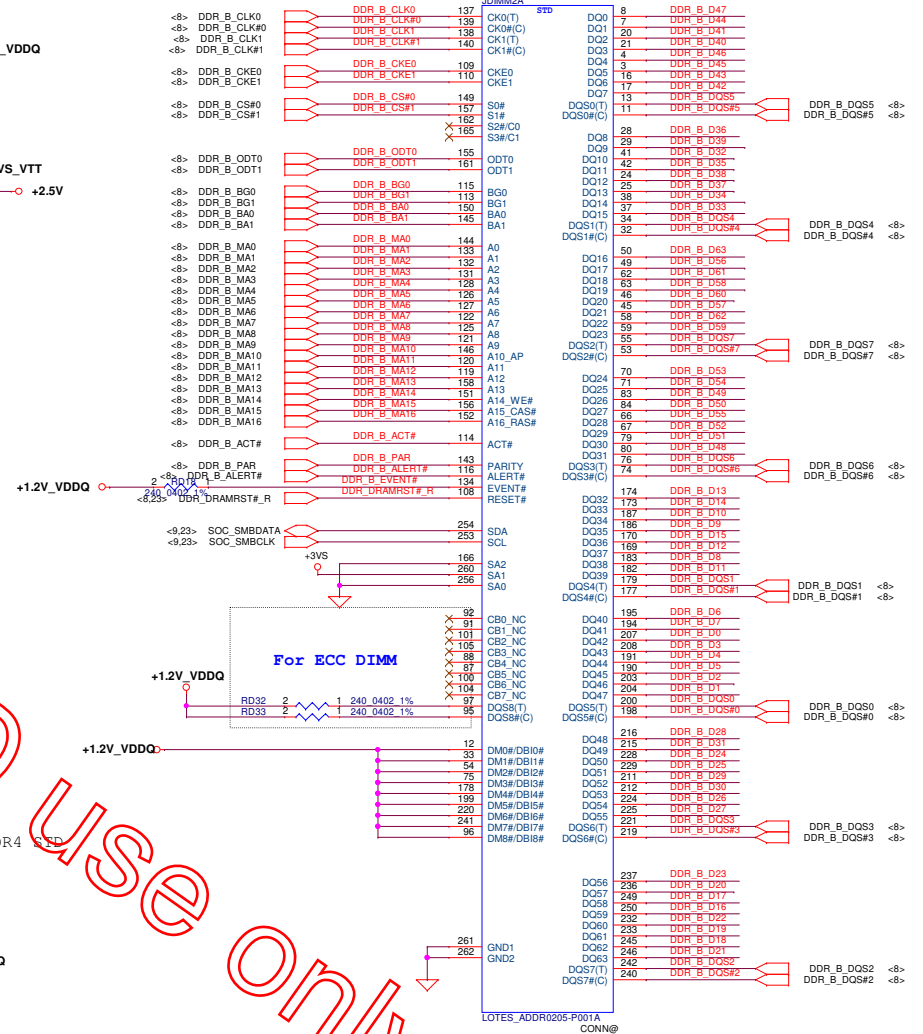
EMC CAPS-PLACE
< 4mm from SO-DIMM VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)



follow RVP 1p0
10uF*8
1uF*8
@330uF*1



Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 8GB



Security Classification			Compal Secret Data		2022/08/05		Title		Compal Electronics, Inc.	
Issued Date			2021/08/05		Deciphered Date		2022/08/05		Title	
									DDRV CHB: DIMM0	
									Size	
									Document Number	
									HH5A4 MB LA-M211P	
									Rev	
									1A	
									Date	
									Monday, April 18, 2022	
									Sheet	
									24 of 122	

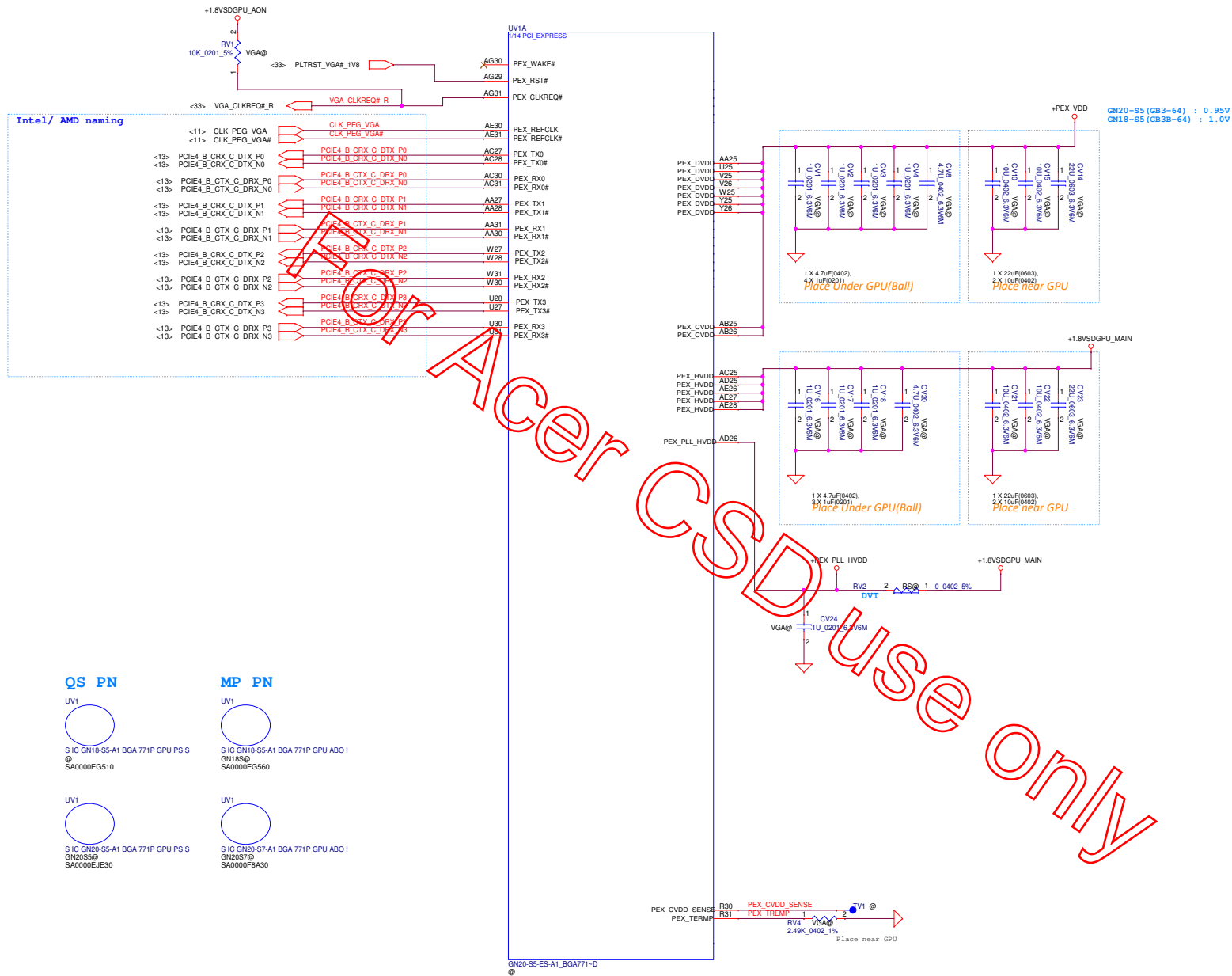
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Main Func = Nv - MEMORY: GPU Partition A/B

Table 3.11 GB3-64, GB3B-64 Power Rail Filtering

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU		Filtering near GPU			
			Footprint	BOM ¹	Value ²	Footprint	BOM ¹	Value ²
FB_PLLVDD	2	1.8V	2	2	10F (1 per ball)	1	1	300 bead
						1	1	22uF
						2	2	4.7uF

Security Classification Compal Secret Data

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Document Number NV(2/10)-GPU VRAM

Size HHS44 MB LA-M211P

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Main Func = Nv - MEMORY: GPU Partition A/B

20mil

50 mils

Table 3.11 GB3-64, GB3B-64 Power Rail Filtering

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU		Filtering near GPU		
			Footprint	BOM ¹	Footprint	BOM ¹	Value ²
FB_PLLVDD	2	1.8V	2	2	10F (1 per ball)	1	300 bead
						1	22uF
						2	4.7uF

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Main Func = Nv - MEMORY: GPU Partition A/B

Table 3.11 GB3-64, GB3B-64 Power Rail Filtering

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU		Filtering near GPU			
			Footprint	BOM ¹	Value ²	Footprint	BOM ¹	Value ²
FB_PLLVDD	2	1.8V	2	2	10F (1 per ball)	1	1	300 bead
						1	1	22uF
						2	2	4.7uF

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Table 3.11 GB3-64, GB3B-64 Power Rail Filtering

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU		Filtering near GPU			
			Footprint	BOM ¹	Value ²	Footprint	BOM ¹	Value ²
FB_PLLVDD	2	1.8V	2	2	10F (1 per ball)	1	1	300 bead
						1	1	22uF
						2	2	4.7uF

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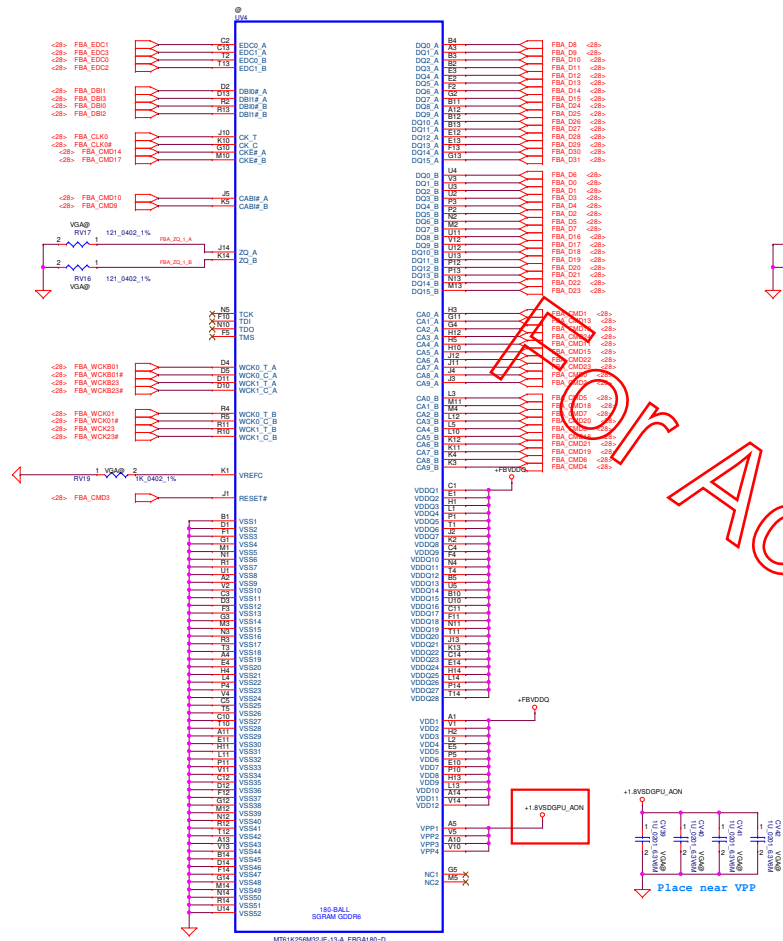
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NV(2/10)-GPU VRAM

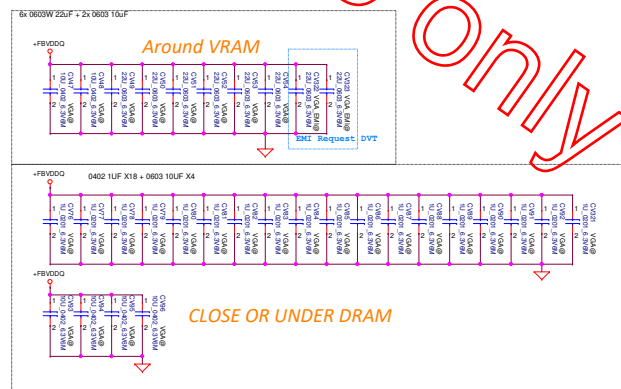
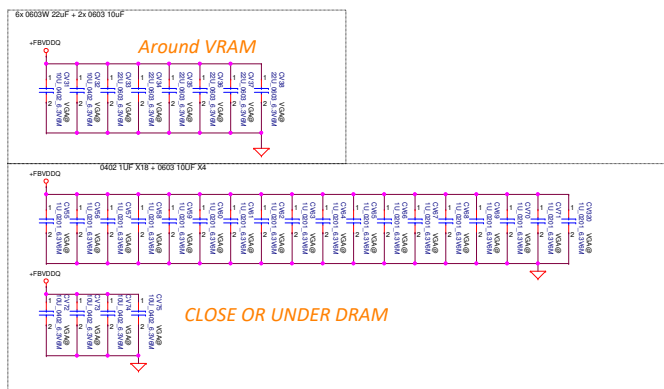
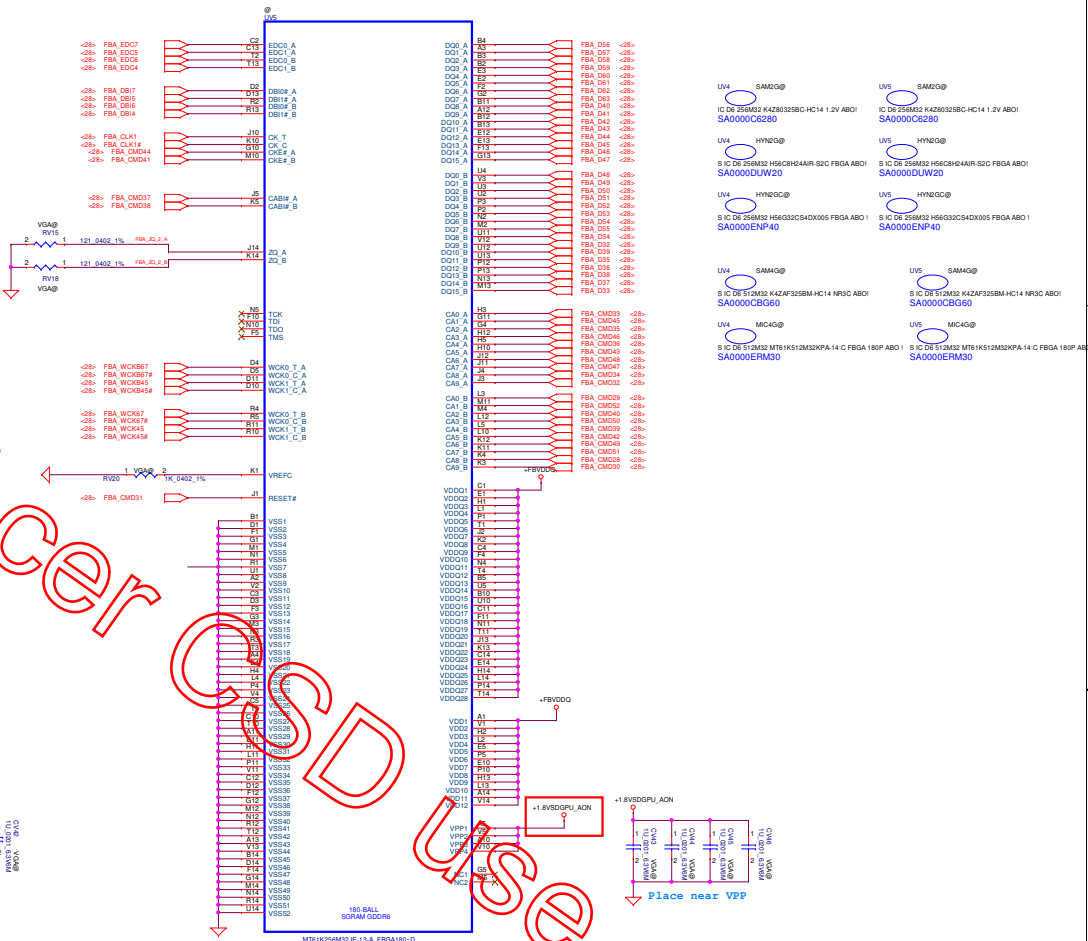
Size Document Number **HH544 MB LA-M211P** **Rev** 1A

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MEMORY: FBA Partition 31..0

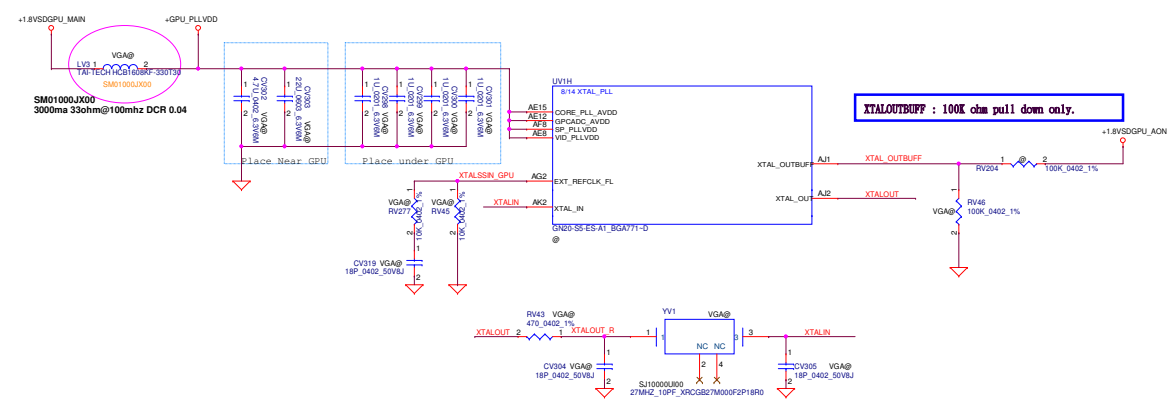
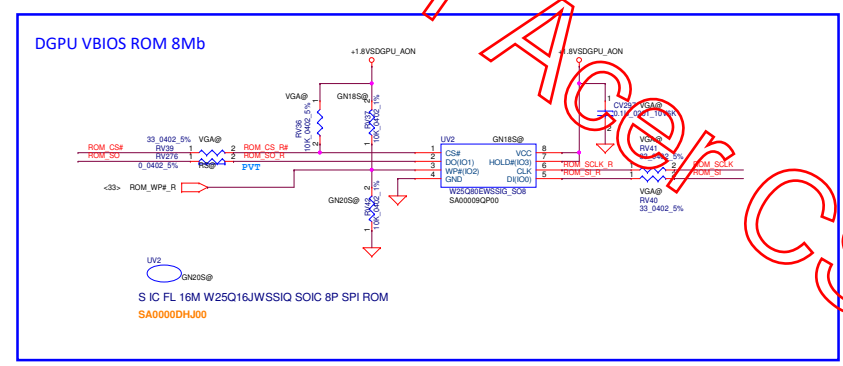
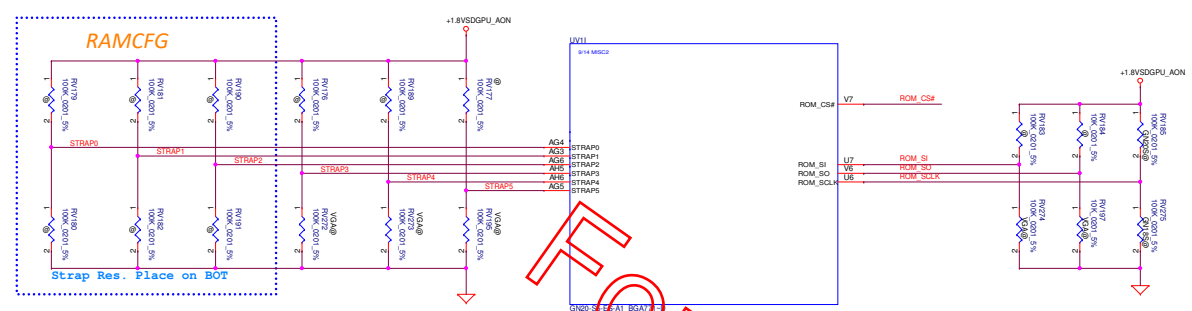


MEMORY: FBA Partition 63..32





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ZZZ GN18X76H4G@
GN18 X76 VRAM HYN 2G
X76954BOL03
ZZZ GN18X76S2G@
GN20 X76 VRAM SAM 2G
X76954BOL04
ZZZ X76H4G@
GN18 X76 VRAM HYN 2G C-Die
X76954BOL07
ZZZ GN20X76H4G@
GN20 X76 VRAM HYN 2G
X76954BOL05
ZZZ GN20X76S2G@
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X76954BOL06
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X76954BOL08
ZZZ GN20X76H4G@
GN20 X76 VRAM SAM 4G
X76954BOL11
ZZZ GN20X76S4G@
GN20 X76 VRAM SAM 4G
X76954BOL12

8Gb VRAM	Strap 0	Strap 1	Strap 2
SAMSUNG (0x0)	L	L	L
HYUNIX (0x2)	L	H	L
HYUNIX C-Die (0x5)	H	L	H

16Gb VRAM	Strap 0	Strap 1	Strap 2
SAMSUNG (0x9)	L	M	L
MICRON (0x7)	H	H	H

Table 5. GN20-S5 and GN18-S5 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V ¹	Samsung	K4ZAF325BM-HC14	M-die	0x9	14 Gbps	2028	Full	Production candidate	ES or later	
			Micron	MT61K512M32KPA-14:C	C-die	0x7	14 Gbps	N/A	Full	Post-production candidate	TBD	
			Hynix	TBD	TBD	0x8	14 Gbps	N/A	Full	Post-production candidate	TBD	
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V ¹	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2009	Full	Production candidate	ES or later	
			Hynix	H56C8H24AIR-52E	A-die	0x2	14 Gbps	N/A	Full	Production candidate	QS or later	
			Hynix	H56G32CSA7W005	C-die	0x5	16 Gbps	N/A	Full	Production candidate	PS or later	

Notes:
¹ Refer to GN20-S5 and GN18-S5 GeForce GPU Product Spec for memory voltages and clocks.
For GN20-S5 and GN18-S5, the maximum allowable memory case temperature is 95 °C.

(GN20-S5) Straps setting => Follow below settings.

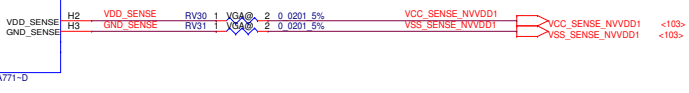
ROM_SO_ (10K)	ROM_SI_	ROM_SCLK_	Strap5_	Strap4_	Strap3_	Strap2_	Strap1_	Strap0_
L	L	H	L	L	L	RVL	RVL	RVL

(GN18-S5) Straps setting => Follow below settings.

ROM_SO_ (10K)	ROM_SI_	ROM_SCLK_	Strap5_	Strap4_	Strap3_	Strap2_	Strap1_	Strap0_
L	L	L	L	L	L	RVL	RVL	RVL

Table 1.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0	(0x0000)
L	L	H	1	(0x0001)
L	H	L	2	(0x0002)
L	H	H	3	(0x0003)
H	L	L	4	(0x0004)
H	L	H	5	(0x0005)
H	H	L	6	(0x0006)
H	H	H	7	(0x0007)
L	L	M	8	(0x0008)
L	M	L	9	(0x0009)
L	M	H	10	(0x000A)
L	H	M	11	(0x000B)
M	L	L	12	(0x000C)
M	L	H	13	(0x000D)



+FBVDDQ



Rail	Balls	Voltage	Filtering under GPU
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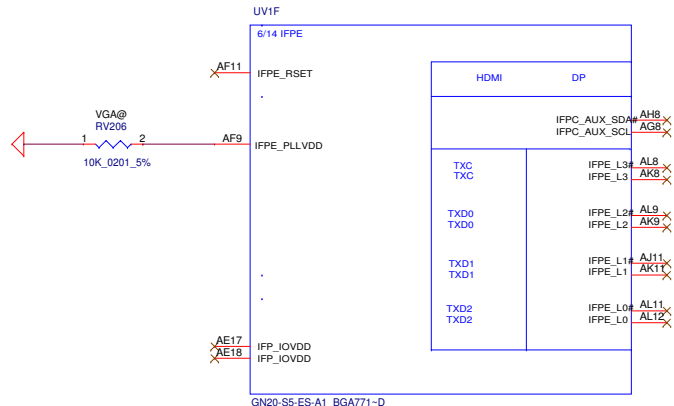
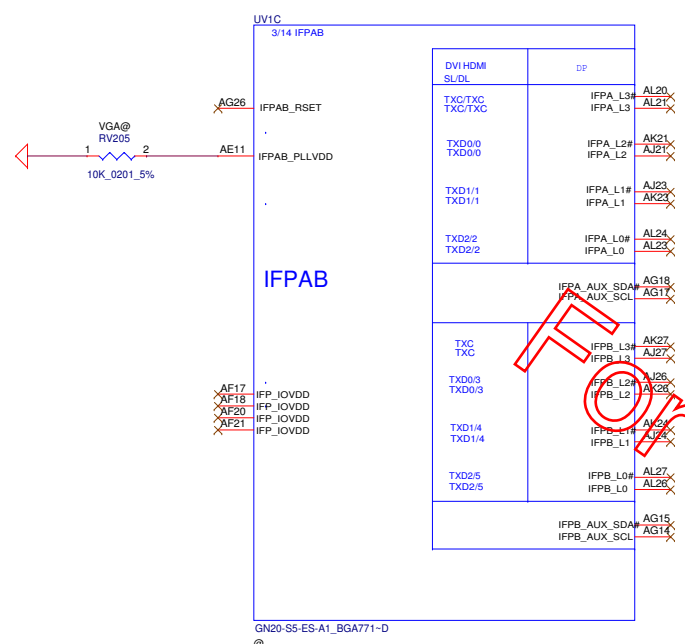
		1.200					
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Rail	Balls	Voltage	Filtering under GPU
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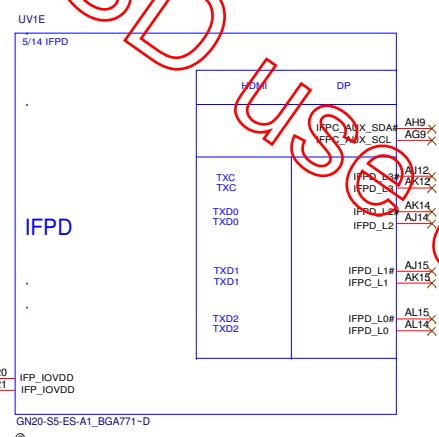
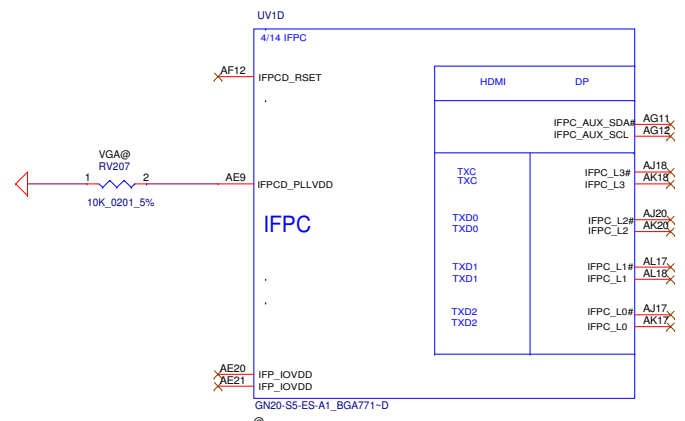
A horizontal timeline bar with vertical tick marks for each year from 2014 to 2017. The years are labeled below the bar: 2014, 2015, 2016, 2017. Above the bar, a box labeled 'Study' spans from 2014 to 2017. Below the bar, a box labeled 'Data collection' spans from 2014 to 2015. A box labeled 'Analysis' spans from 2016 to 2017. A box labeled 'Publication' spans from 2017 to 2018.

Main Function:Nv - IFP ABCD



7.2 Unused pins

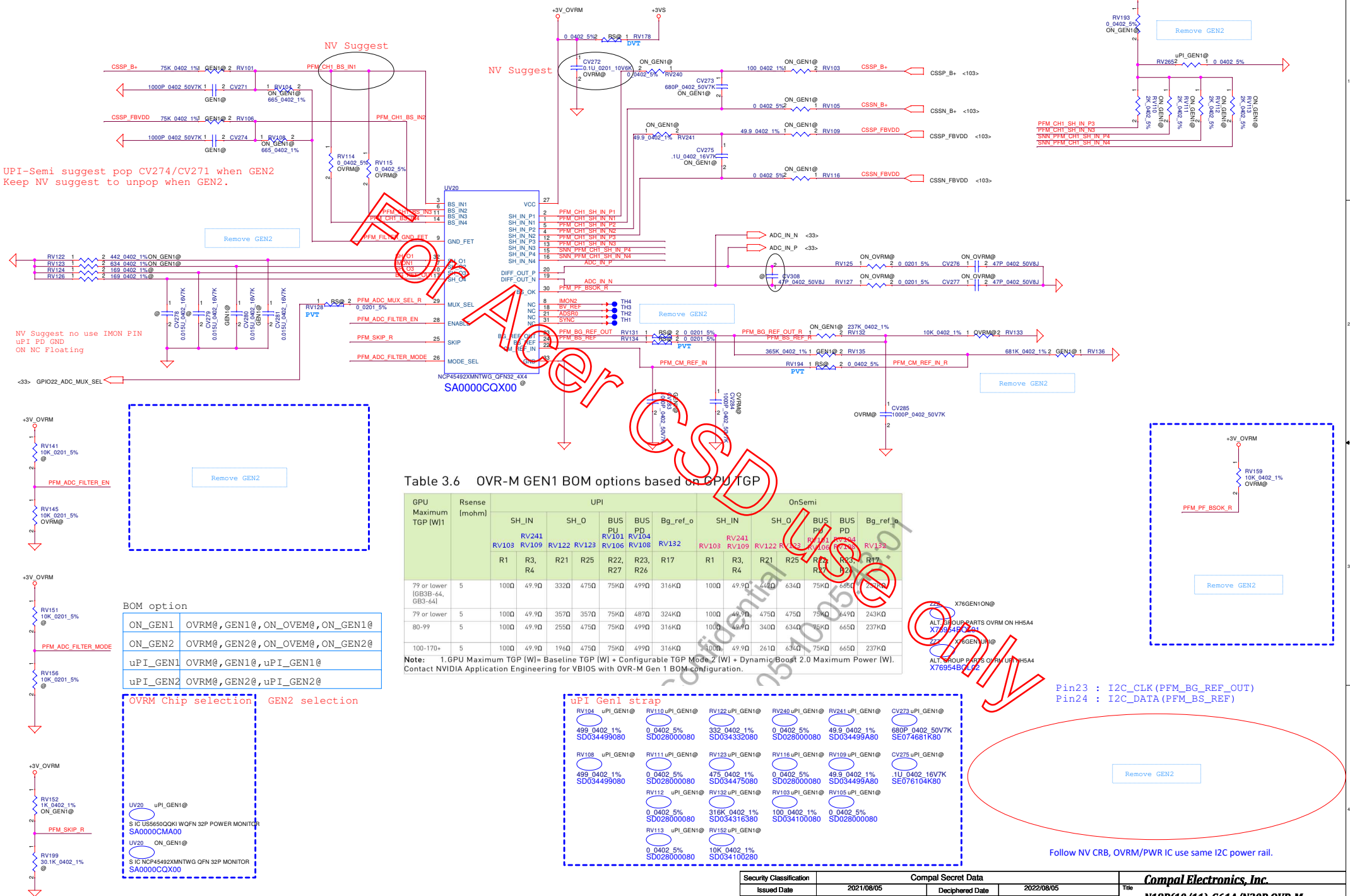
If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RESET (xy = AB,CD,EF) can be left unconnected and IFPxy_PLLVDD should be 10K PD to GND if neither of IFPx/IFPy is in use. For example, if neither link of the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD must be 10K PD to GND, IFPAB_RESET should be left unconnected, and all signals and references associated with Link A and Link B should also be left unconnected. IFPxy_I/OVDD rail can be left unconnected if no IFP link is used. If any IFP is used, all IFP_I/OVDD rails must be connected to power rail.



OVR-M GEN1

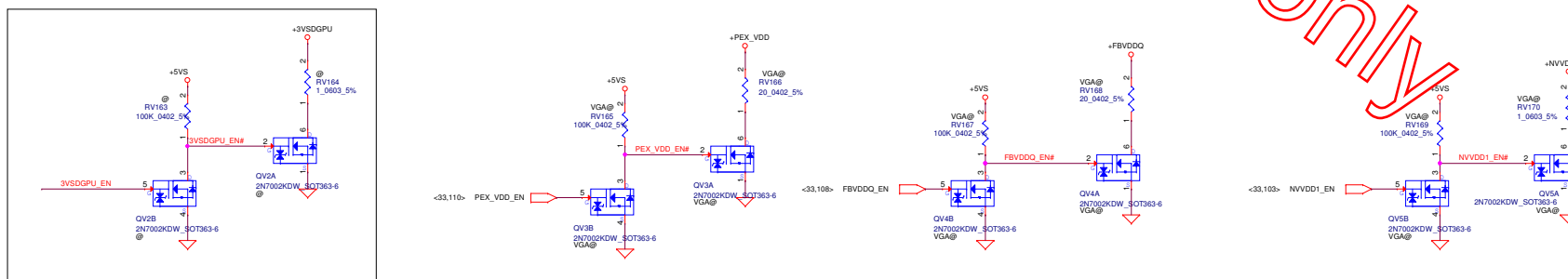
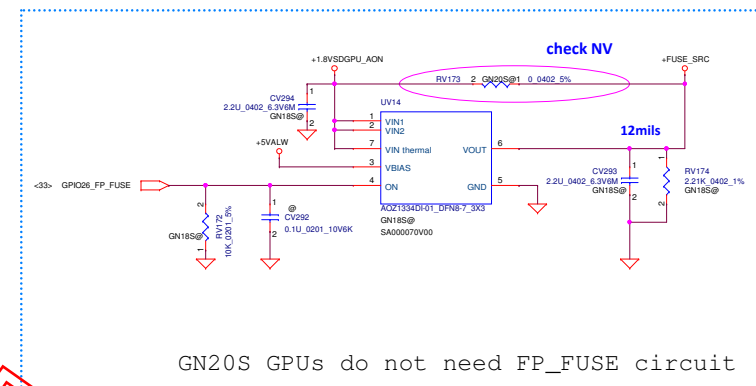
For OVRM Keep ON

GEN2 NV suggest BS_IN3,4 need also connect with BS_IN2 (CSSP_FBEVDD)
No use SH_P/N need PU the same voltage as no use BS_IN



Follow NV CRB, OVRM/PWR IC use same I2C power rail.

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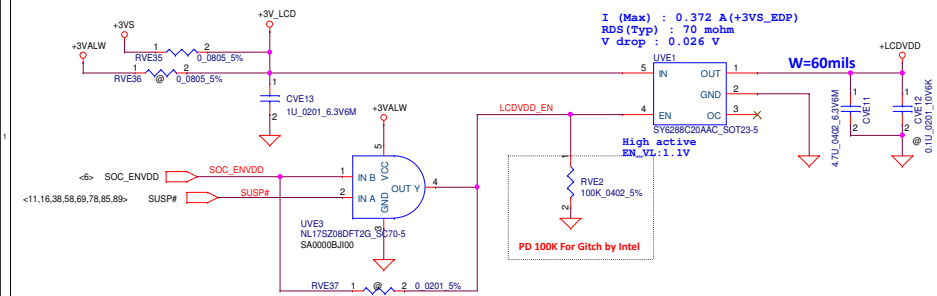
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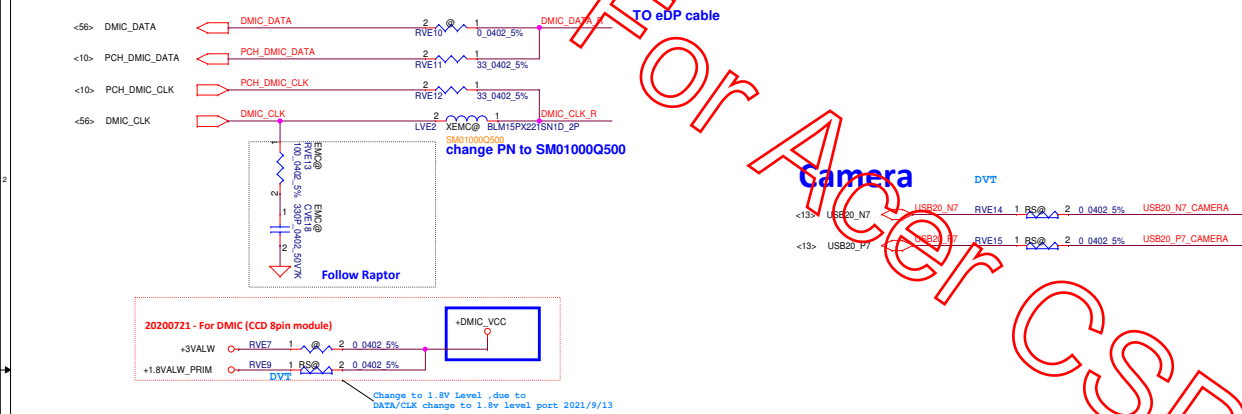
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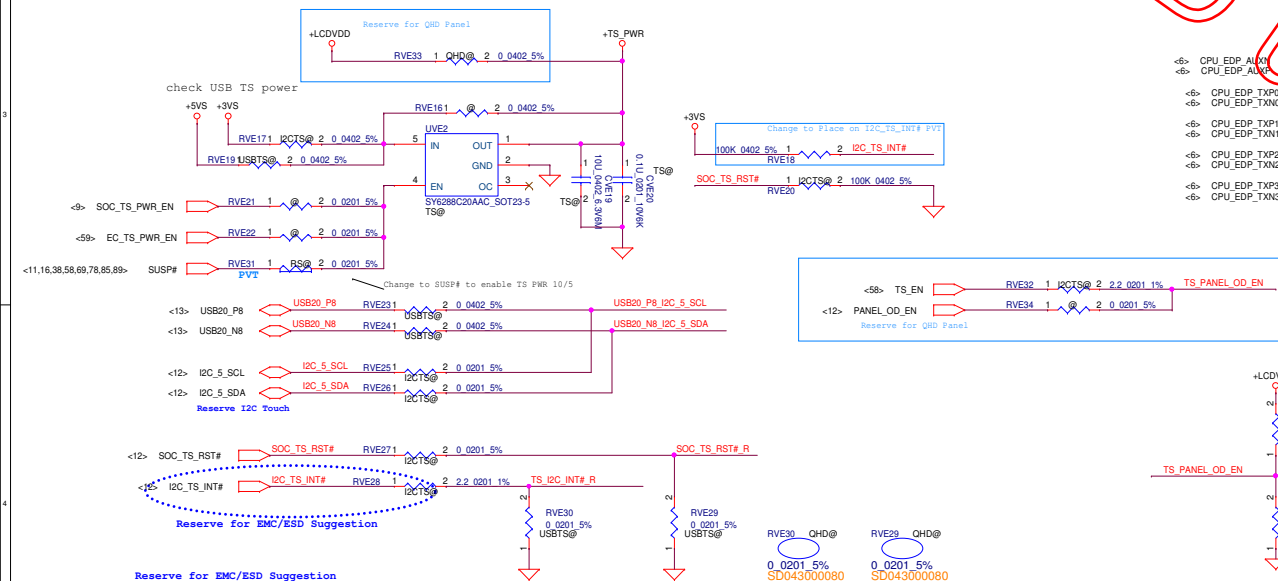
LCD POWER CIRCUIT



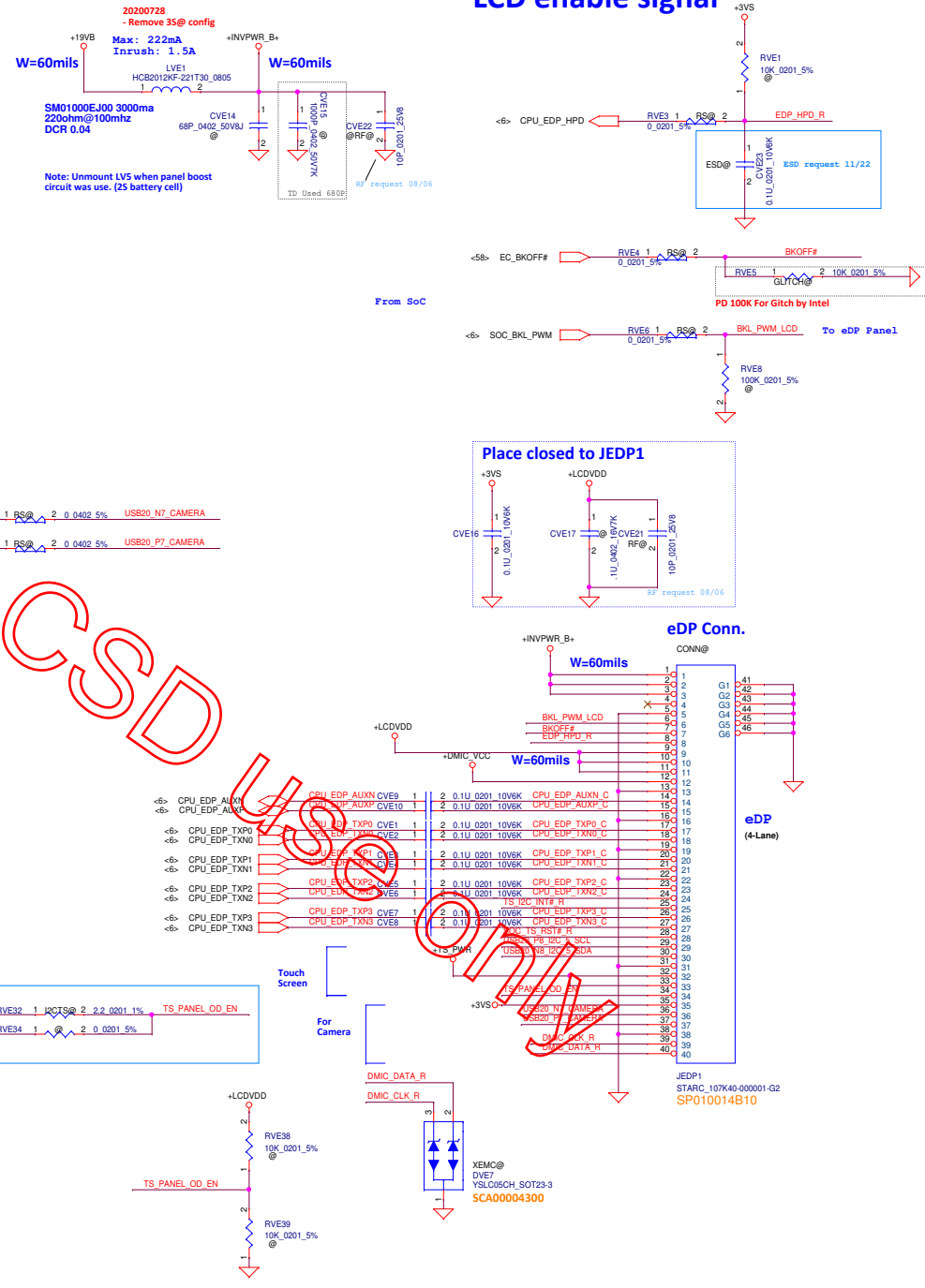
DMIC



USB/I2C Touch Screen Co-Lay



LCD enable signal

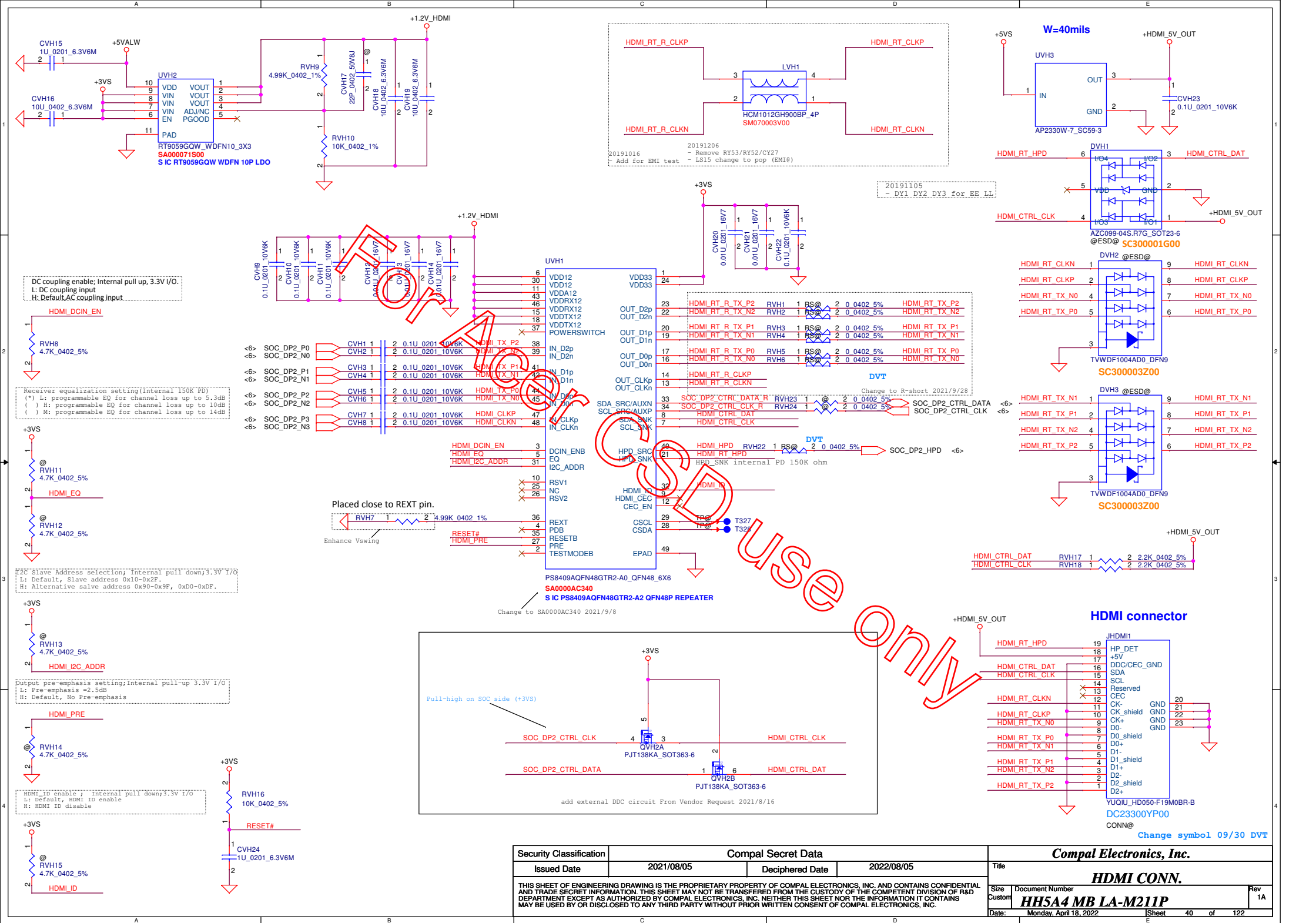


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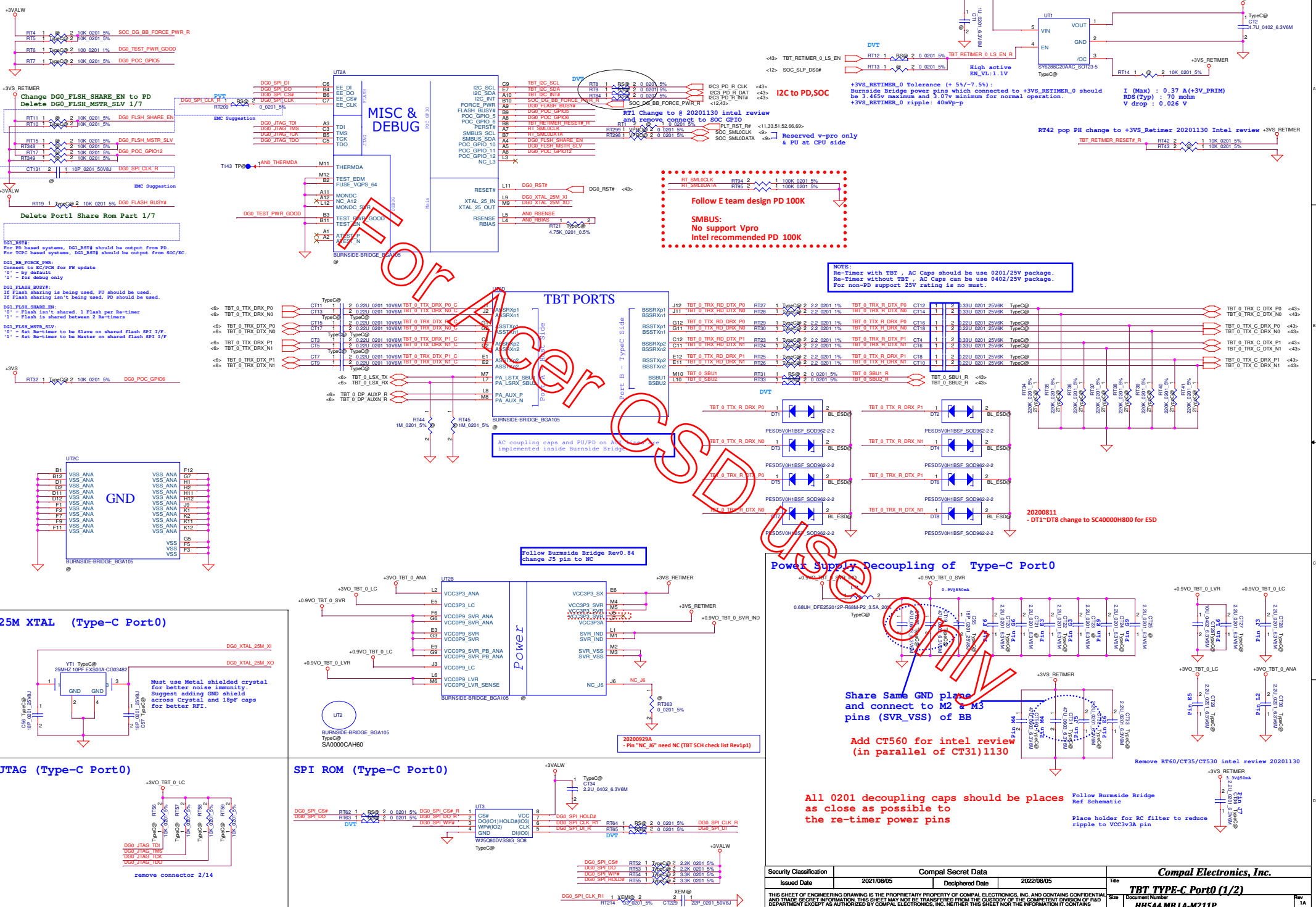
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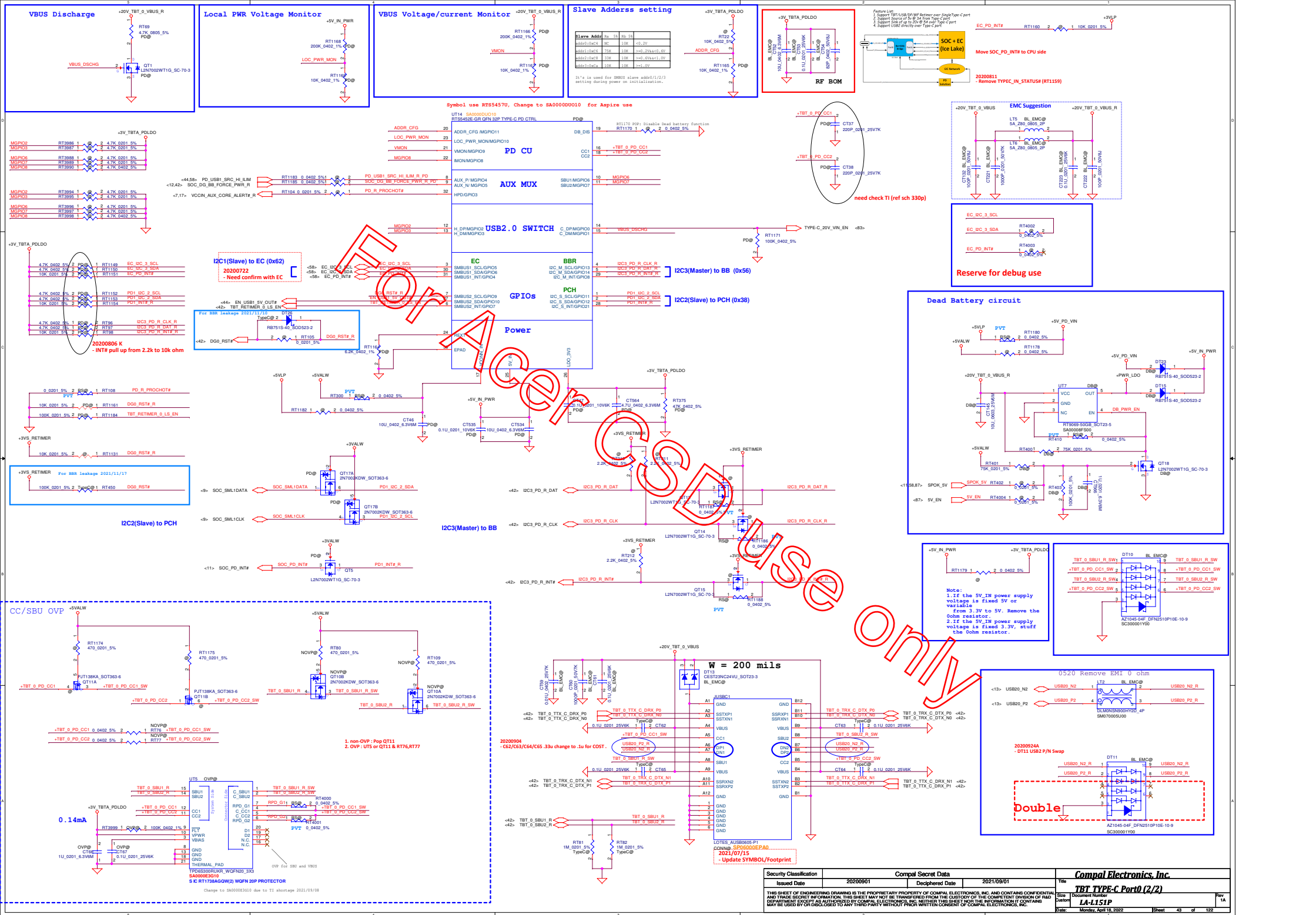


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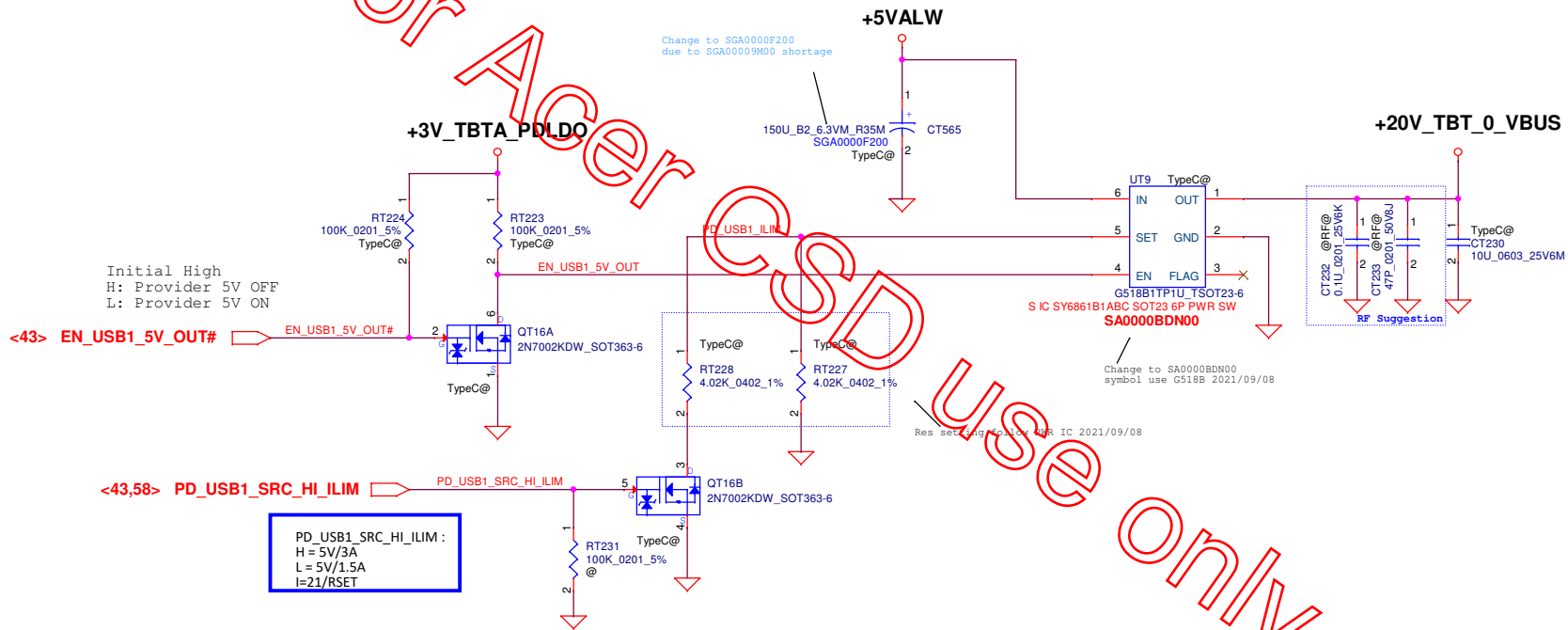
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MB_USB3.1 TypeC Conn. (Port 0/ Re-Timer Master)





MB_USB3.1 TypeC Conn. (Power Path)
- For Realtek 5452E



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					HH5A4 MB LA-M211P
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				Rev	1A

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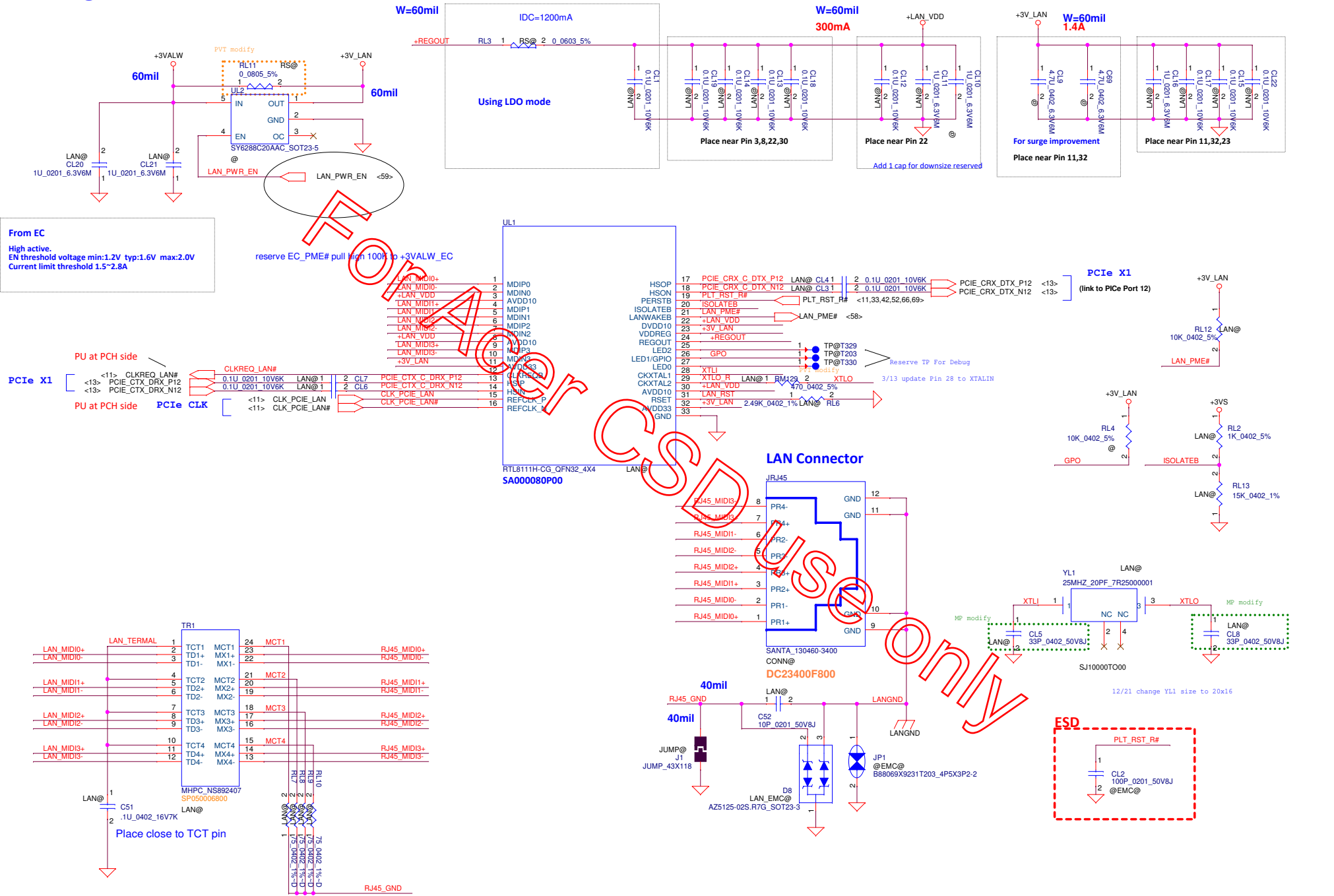
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					HH5A4 MB LA-M211P
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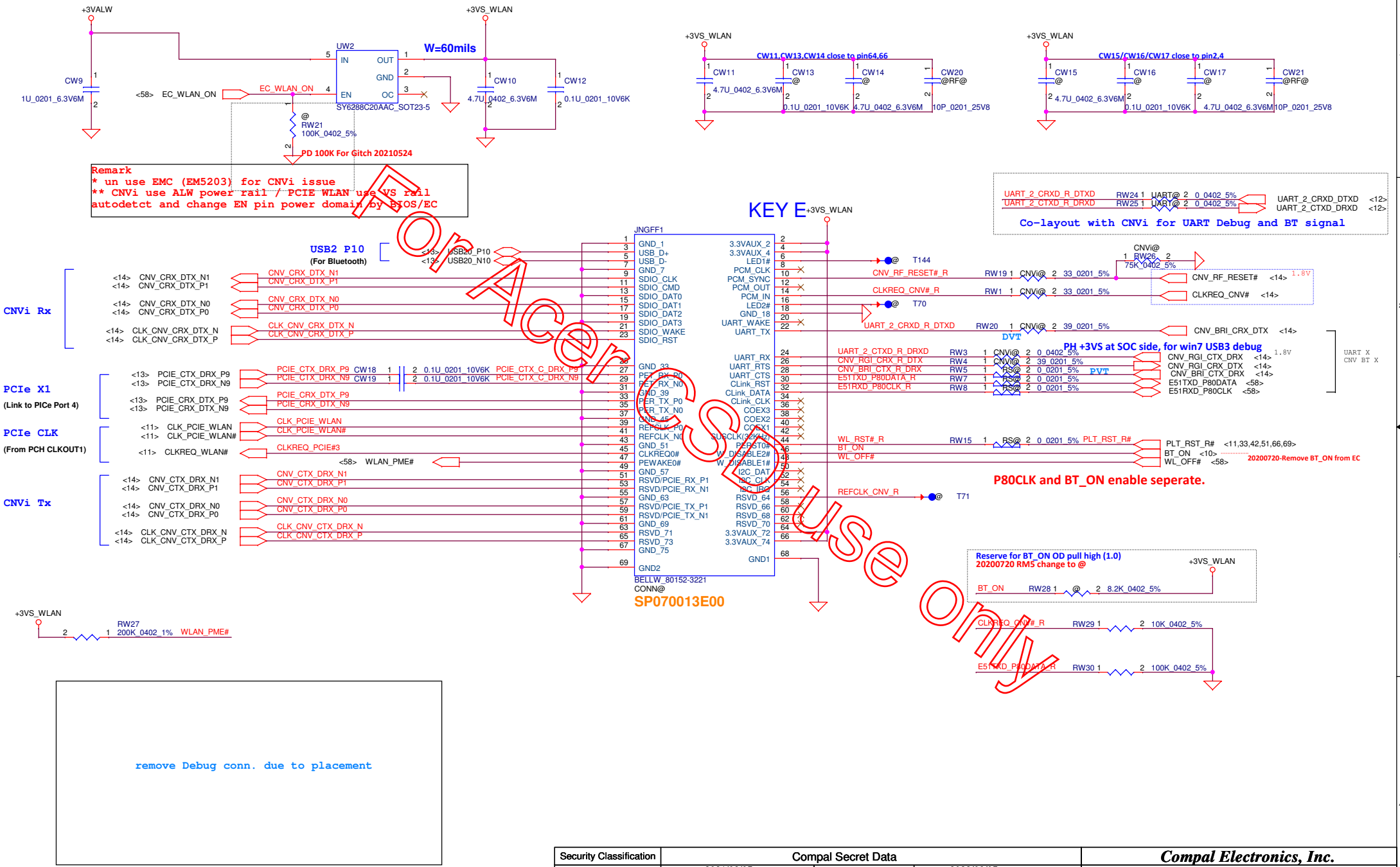
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LAN-RTL8111H



NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



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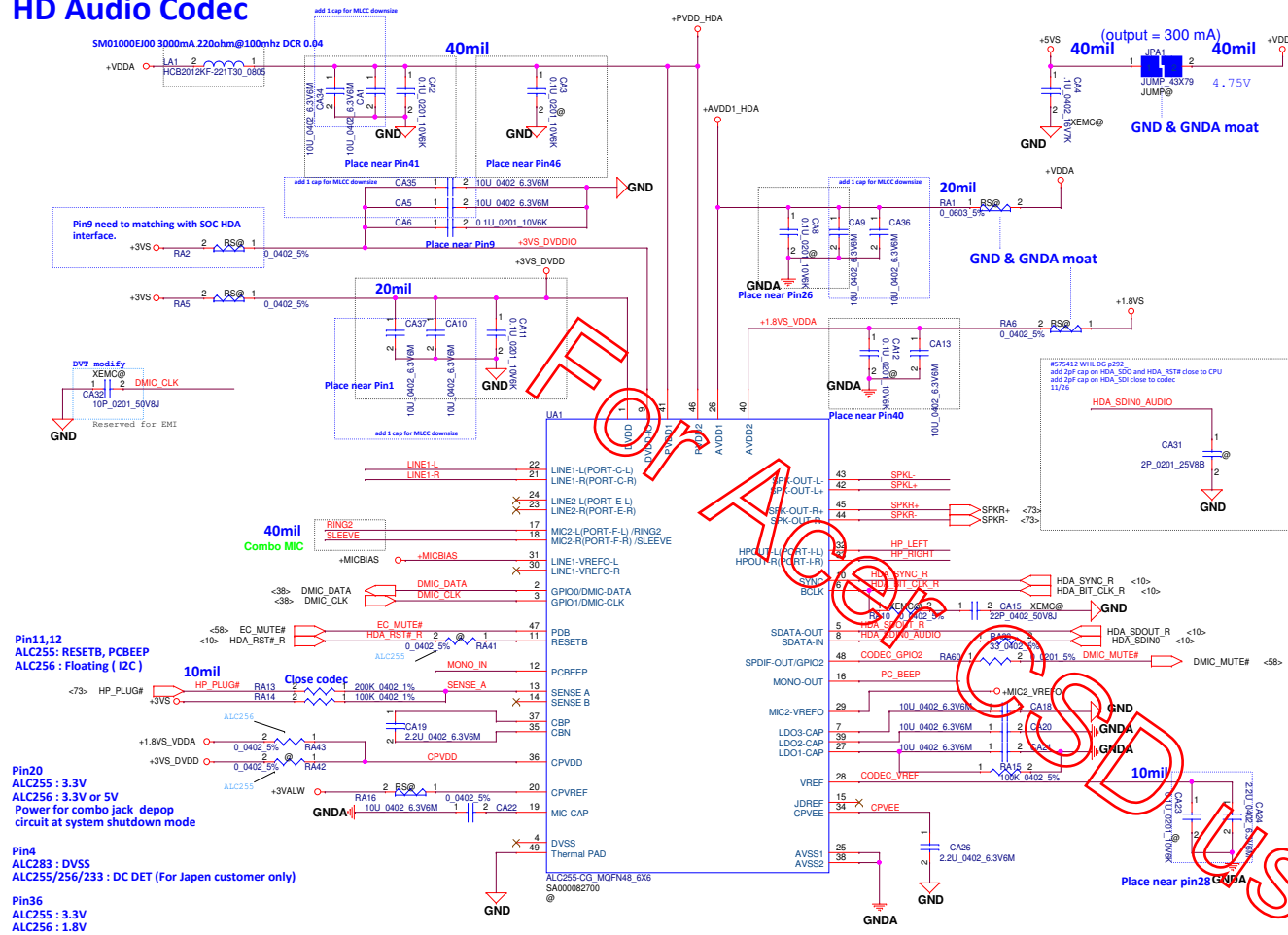
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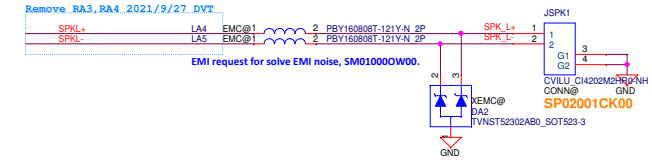
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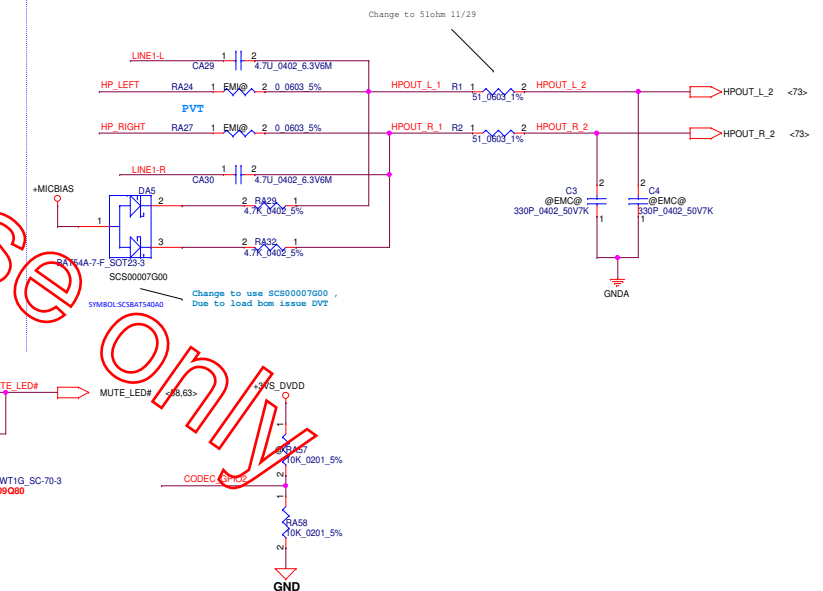
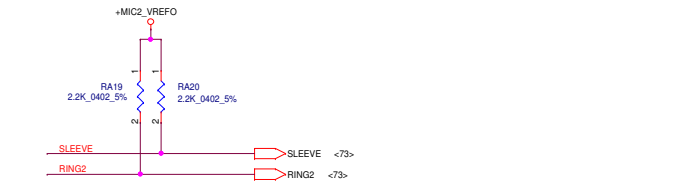
HD Audio Codec



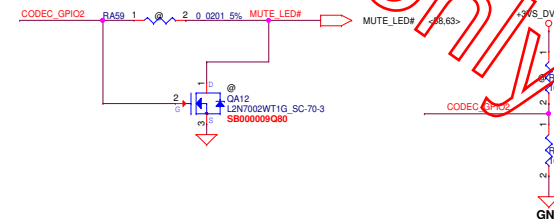
Int. Speaker Conn.



Headphone Out



Mute LED circuit



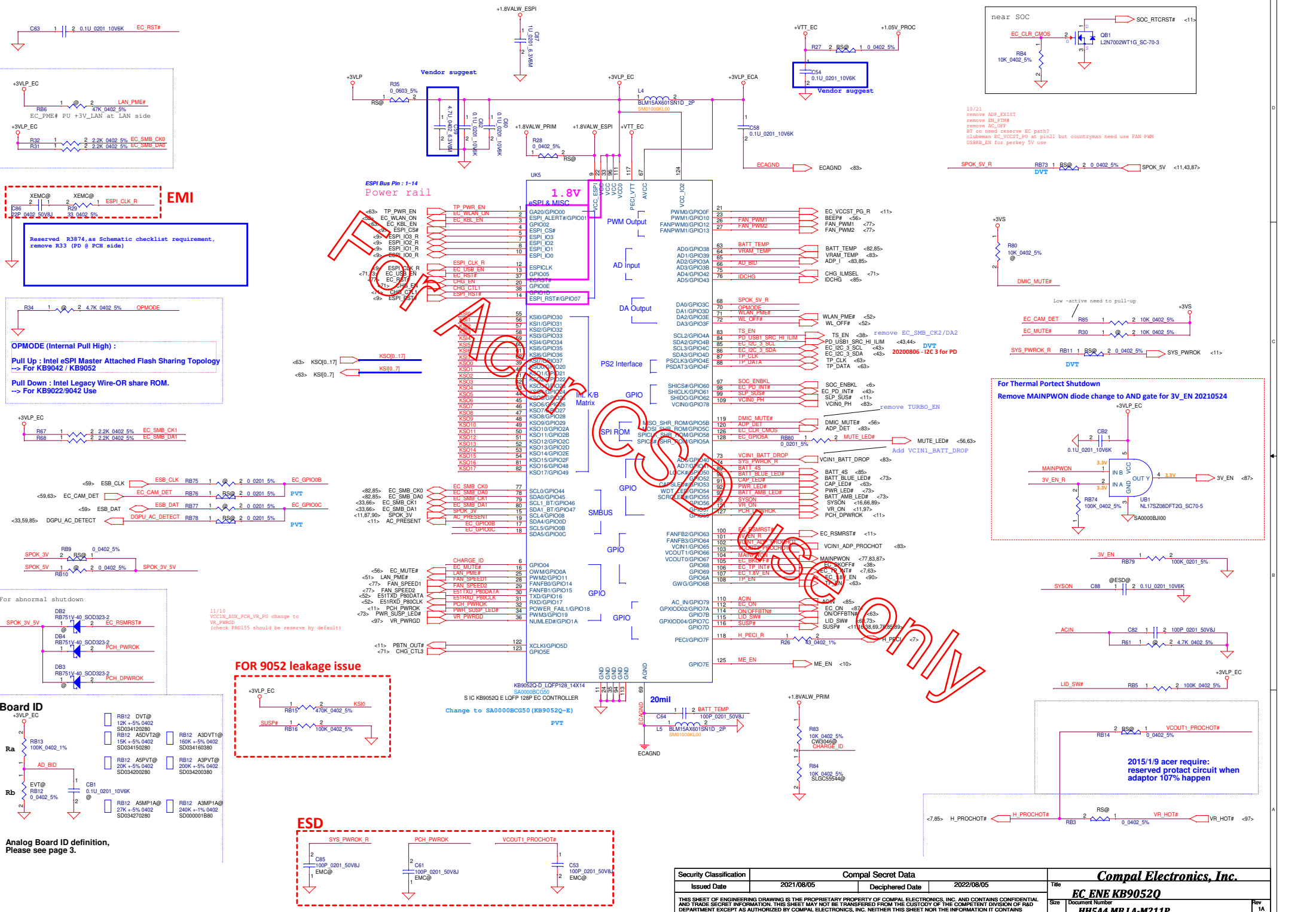
Vendor suggest:
At least one Ground short close to codec.

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				HH5A4 MB LA-M211P	1A
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Title		EC ENE KB9052Q	
Size	Document Number	HHS44 MB LA-M211P	
Date	Monday, April 16, 2022	Sheet	58 of 122

OMEN New ESB CLK&DAT for Extend I/O

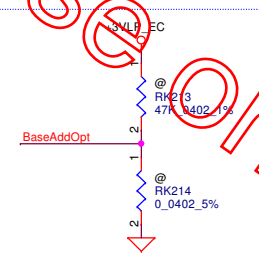
*NMI_DBG#: is a debug pin for EC to
infrom BIOS after press hot key.



Need EC confirm

[GPIO11/BaseAddOpt]
If support second 3810,
please let one 3810 GPIO11 connect GND and
the other keep NC or initial High

- High/NC: USR_EGPIOBaseSetting - 0x00
- Low: USR_EGPIOBaseSetting - 0x08



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				Date:	Monday, April 18, 2022
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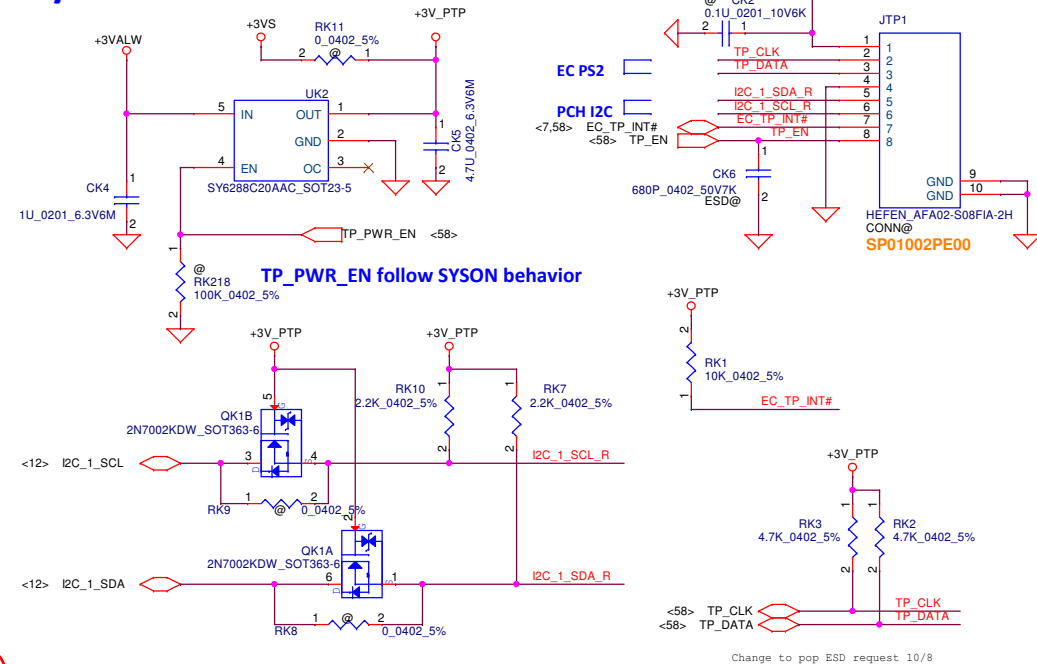
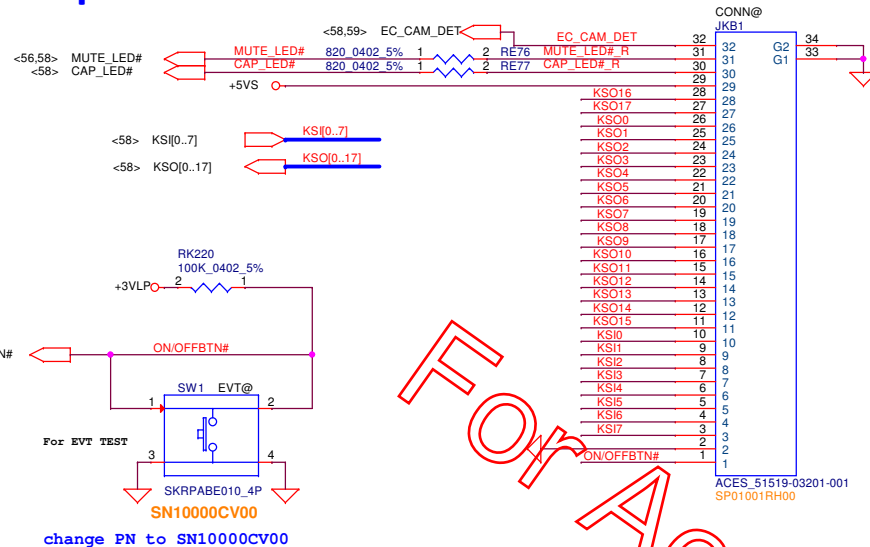
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Title		Reserve for SMB/I2C Block Diagrams			
Size		Document Number			
		HH5A4 MB LA-M211P			
Date:		Monday, April 18, 2022		Sheet 61 of 122	
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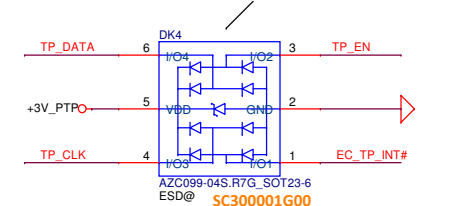
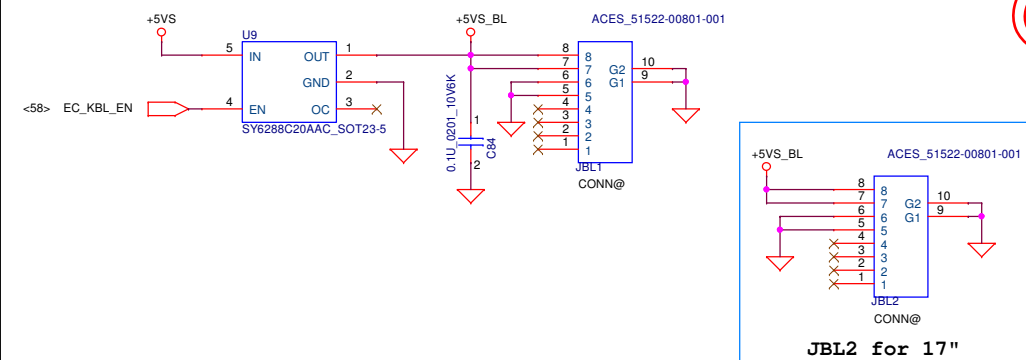
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				Document Number	Rev
				HH5A4 MB LA-M211P	1A
Date: Monday, April 18, 2022				Sheet	62 of 122

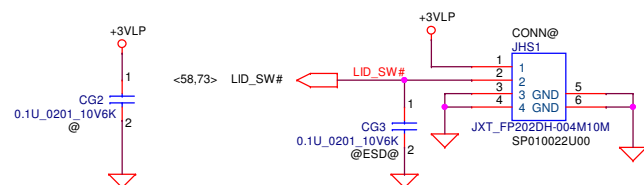
TP/B Conn.



KB BackLight



Hall sensor



Battery LED

Move to SUB/B

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				Size Custom	Document Number	Rev 1.
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					HH5A4 MB LA-M211P
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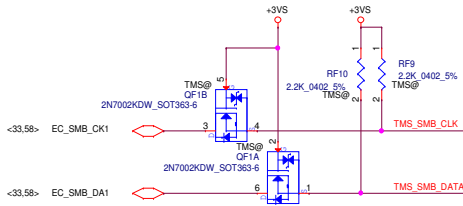
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					HH5A4 MB LA-M211P
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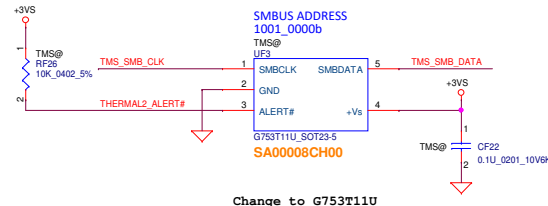
20200717
- Remove G-Sensor

THERMAL SENSOR

20200810
- Check address

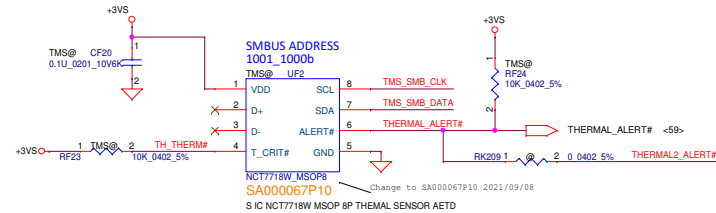


Close to Thermal SKIN

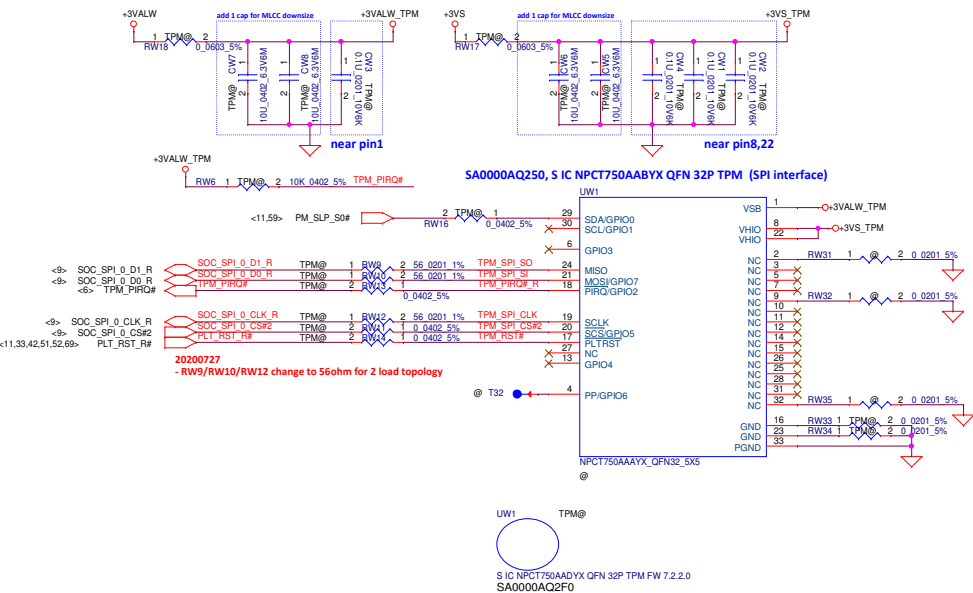


20200928
- Remove 3rd thermal sensor

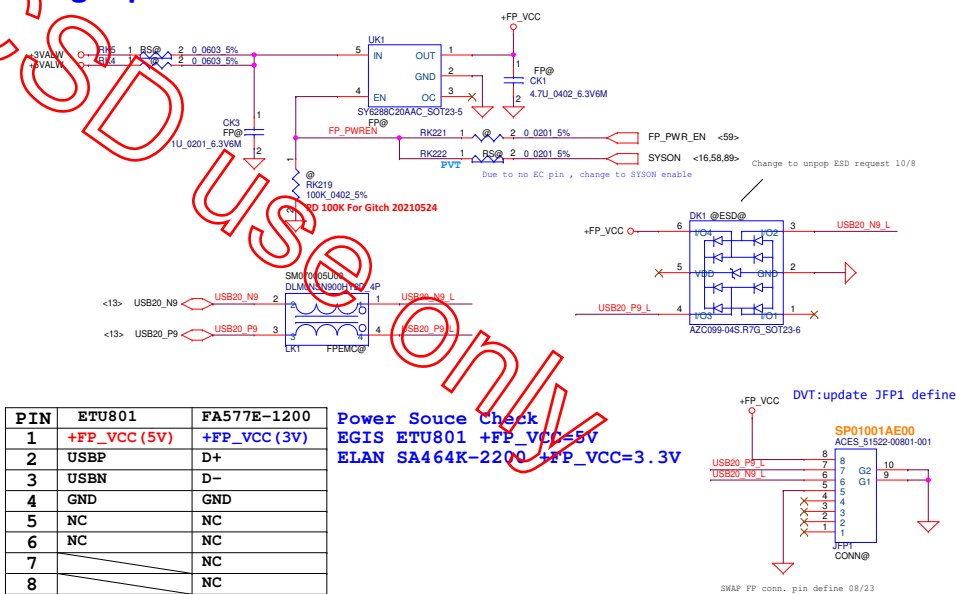
Close to SO-DIMM



TPM 2.0



Finger print

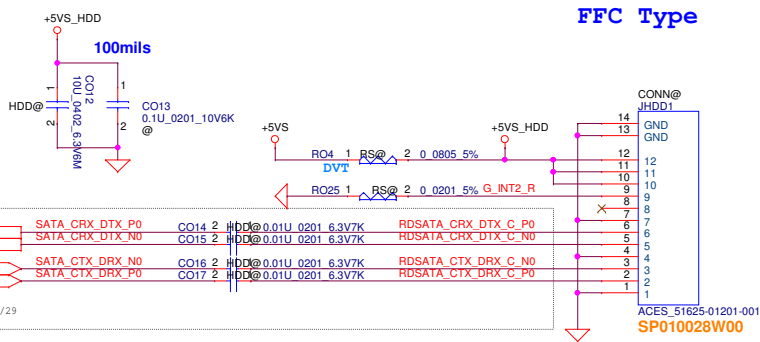


PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

Power Source Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V

Remove SATA Redriver due to length spec

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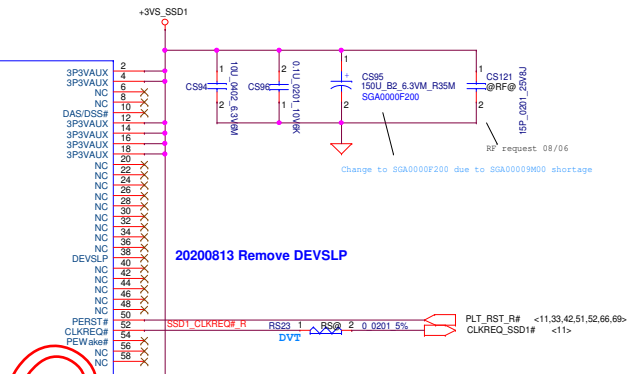
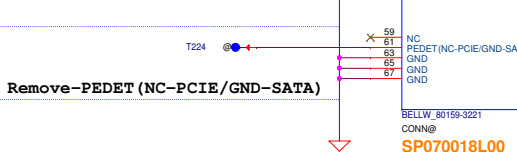
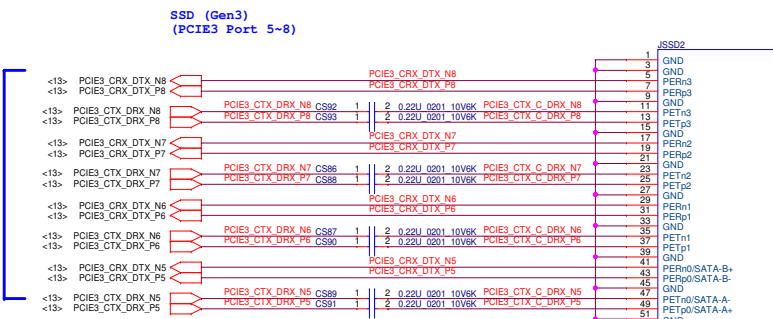
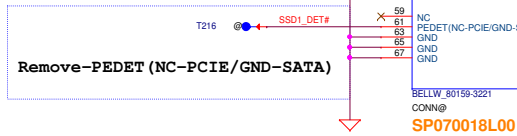
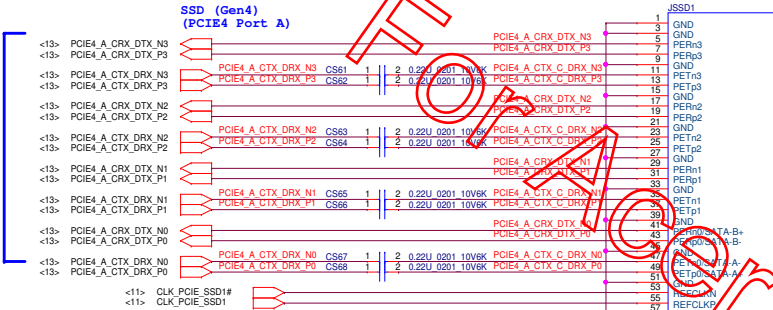
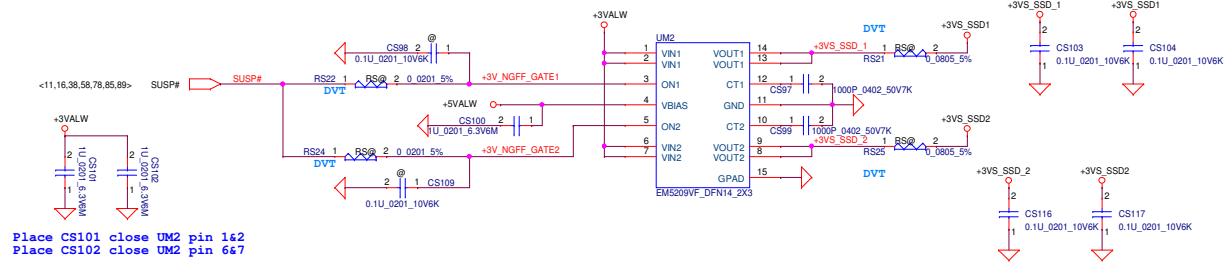


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				HH5A4 MB LA-M211P	1A
				Date: Monday, April 18, 2022	Sheet 67 of 122

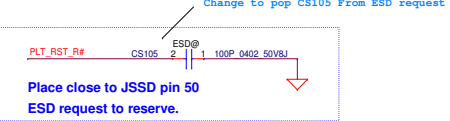
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				Document Number	
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20210517 Power source
> +3VS_SSD1 : JSSD1
> +3VS_SSD2 : JSSD2



20210517 Power source
> +3VS_SSD1 : JSSD1
> +3VS_SSD2 : JSSD2



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		SATA/PCIE-SSD
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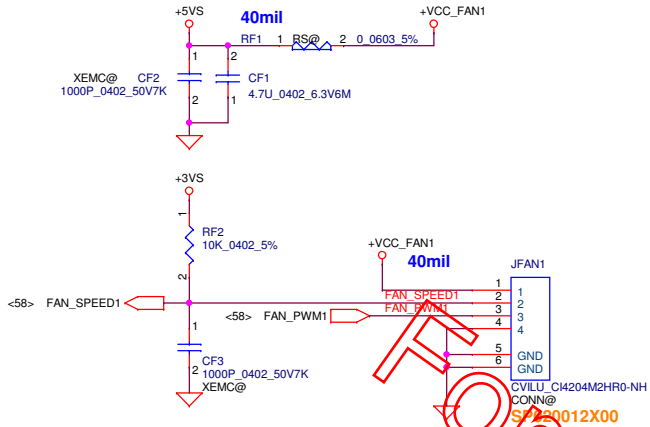
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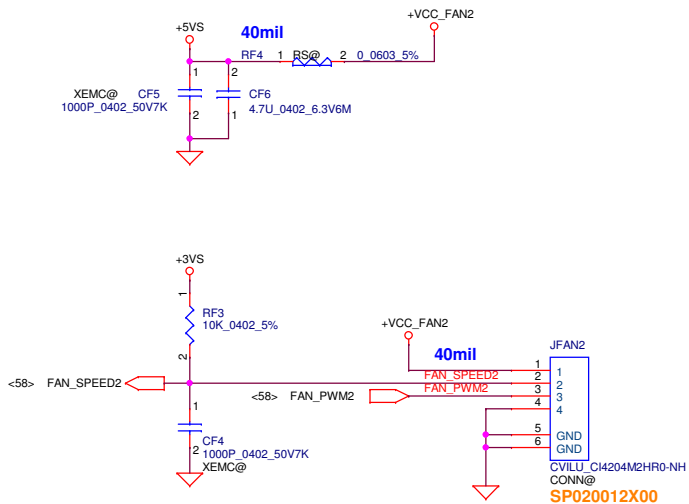
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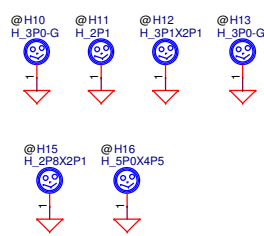
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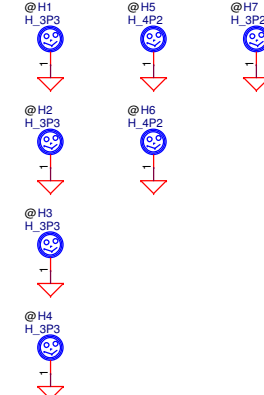
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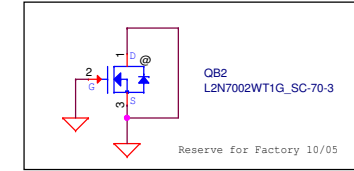
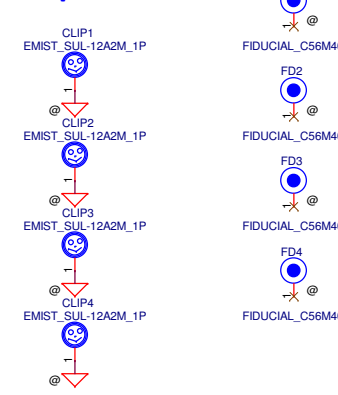
Screw Hole



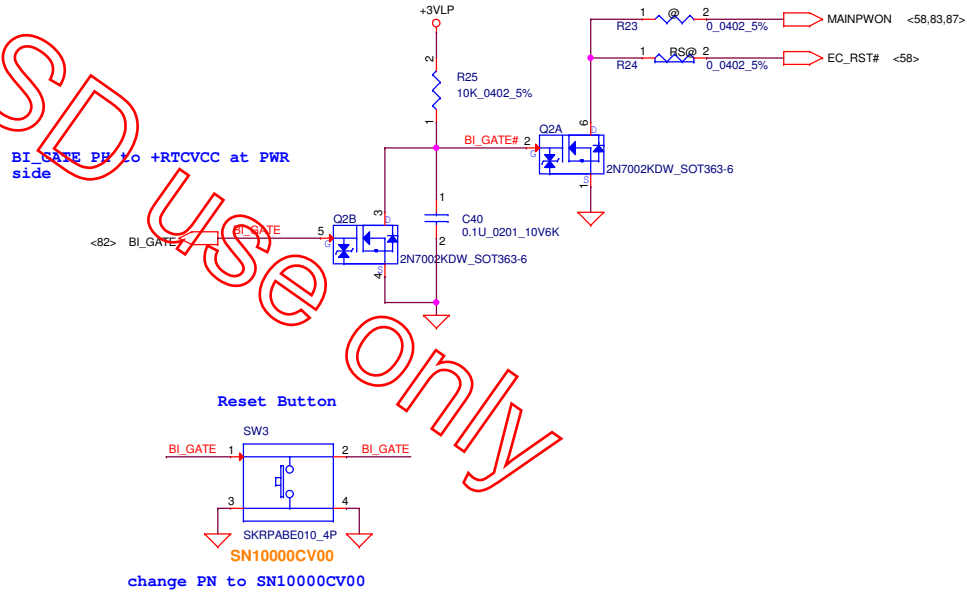
Stand OFF



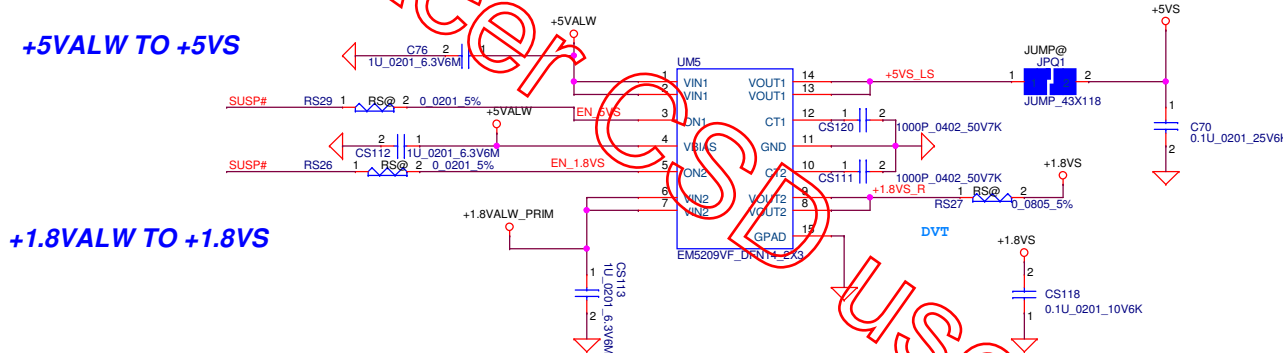
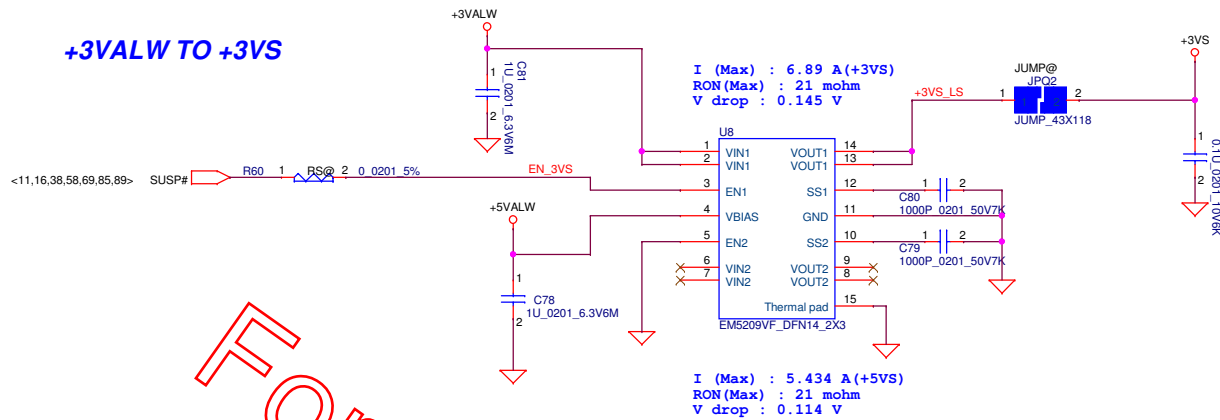
Clips



Reset Circuit



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20200717
- Remove VGA Power sequence

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CPU PN

<p>UC1</p> <p>S IC FJ8071504661126 QY4Y Q0 1G BGA S QY4Y@ SA0000ERH10</p>	<p>UC1</p> <p>S IC FJ8071504661124 QY4W Q0 1G BGA S QY4W@ SA0000ERL00</p>	<p>UC1</p> <p>QS P28W</p> <p>S IC FJ8071504787906 QYYD K0 1.7G BGA S QYYD@ SA0000F4X10</p>	<p>UC1</p> <p>QS U15W</p> <p>S IC FJ8071504826607 Q0E8 R0 1.7G S Q0E8@ SA0000FB530</p>	<p>UC1</p> <p>Sus-QS</p> <p>S IC FJ8071504786604 Q07M L0 2.1G S 0FA Q07M@ SA0000F9E60</p>	<p>UC1</p> <p>I3-1215U</p> <p>S IC FJ8071504827100 SRLFT R0 1.2G BGA 1744 ABO ! SRLFT@ SA0000FBR80</p>	<p>UC1</p> <p>MP</p> <p>I3-1220P</p> <p>S IC FJ8071504827402 SRLFY R0 1.5G BGA 1744 ABO ! SRLFY@ SA0000FE850</p>
<p>UC1</p> <p>S IC FJ8071504661121 QY4T Q0 1.2G BGA S QY4T@ SA0000EQC10</p>	<p>UC1</p> <p>S IC FJ8071504698605 QXZS J0 1G FCBGA S QXZS@ SA0000EL800</p>	<p>UC1</p> <p>S IC FJ8071504786603 QYY9 K0 2.1G BGA S QYY9@ SA0000F4A10</p>	<p>UC1</p> <p>S IC FJ8071504826802 Q0EP R0 1.3G S Q0EP@ SA0000FB720</p>	<p>UC1</p> <p>S IC FJ8071504787907 Q07Q L0 1.7G S 0FA Q07Q@ SA0000F9F70</p>	<p>UC1</p> <p>I5-1235U</p> <p>S IC FJ8071504826802 SRLFO R0 1.3G BGA 1744 ABO ! SRLFO@ SA0000FB7A0</p>	<p>UC1</p> <p>I5-1240P</p> <p>S IC FJ8071504787907 SRLD9 L0 1.7G BGA 1744 ABO ! SRLD9@ SA0000F9FB0</p>
<p>UC1</p> <p>S IC FJ8071504661122 QY4U Q0 1.2G BGA S QY4U@ SA0000EQD10</p>	<p>UC1</p> <p>S IC FJ8071504698606 QXZT J0 1G FCBGA S QXZT@ SA0000EL920</p>	<p>UC1</p> <p>S IC FJ8071504827402 Q0EU R0 1.5G BGA S Q0EU@ SA0000FE300</p>	<p>UC1</p> <p>S IC FJ8071504827100 Q0EV R0 1.2G BGA S Q0EV@ SA0000FBR00</p>		<p>UC1</p> <p>I7-1255U</p> <p>S IC FJ8071504826607 SRLFP R0 1.7G BGA 1744 ABO ! SRLFP@ SA0000FB5A0</p>	<p>UC1</p> <p>I7-1260P</p> <p>S IC FJ8071504786607 SRLD6 L0 2.1G FCBGA 1744 ABO ! SRLD6@ SA0000FBV40</p>

A5 X4E PN

<p>ZZZ</p> <p>X4EDIS@</p> <p>SMT EMC DIS EE LAM211 HH5A4 X4EAUWBOL01</p>	<p>ZZZ</p> <p>X4EDISNFP@</p> <p>PCBA EMC DIS W/O FP EE LAM211 HH5A4 X4EAUWBOL04</p>
<p>ZZZ</p> <p>X4EUMA@</p> <p>SMT EMC UMA EE LAM211 HH5A4 X4EAUWBOL02</p>	<p>ZZZ</p> <p>X4EUMANFP@</p> <p>PCBA EMC UMA W/O FP EE LAM211 HH5A4 X4EAUWBOL03</p>

A5 X4E PN

<p>ZZZ</p> <p>X4EA3DIS@</p> <p>SMT EMC DIS LAM211 HH5J4 X4EAUWBOL51</p>	<p>ZZZ</p> <p>X4EA3DISNFP@</p> <p>SMT EMC DIS LAM211 HH5J4 X4EAUWBOL56</p>
<p>ZZZ</p> <p>X4EA3UMA@</p> <p>SMT EMC UMA LAM211 HH5J4 X4EAUWBOL52</p>	<p>ZZZ</p> <p>X4EA3UMANFP@</p> <p>SMT EMC UMA W/O FP LAM211 HH5J4 X4EAUWBOL54</p>
<p>ZZZ</p> <p>X4EA3UMAS@</p> <p>SMT EMC UMA SLIM LAM211 HH5J4 X4EAUWBOL53</p>	<p>ZZZ</p> <p>X4EA3UMASNFP@</p> <p>SMT EMC UMA SLIM W/O FP LAM211 HH5J4 X4EAUWBOL55</p>

HDMI LOGO

ZZZ

HDMI LOGO 45@ RO0000003HM

PCB PN

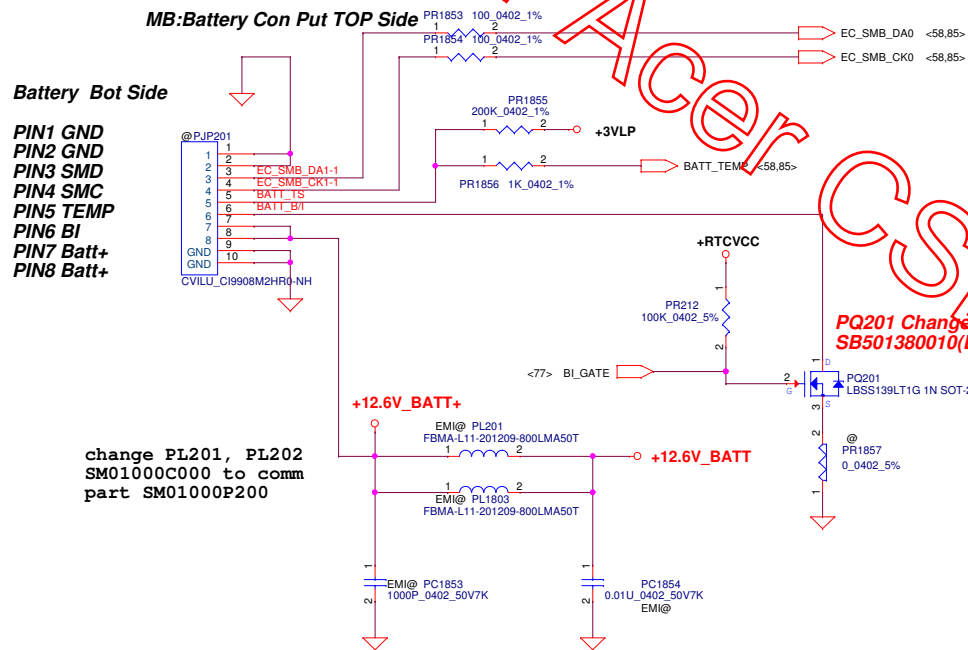
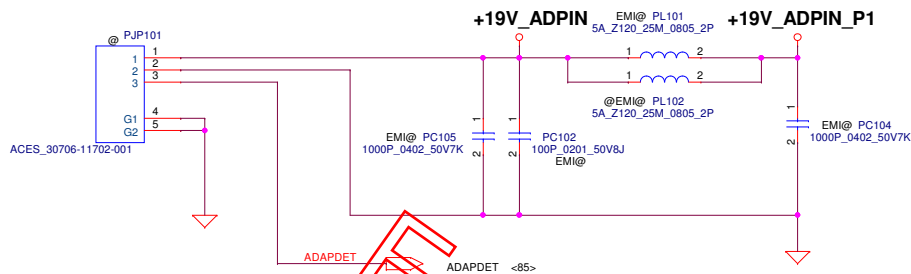
<p>ZZZ</p> <p>PCB 3TY LA-M211P REV0 MB 1 S PCB@ DA8001SW000</p>	<p>ZZZ</p> <p>PCB HH5A4 LA-M211P LS-M211P DAZ10@ DAZ3TY00100</p>	<p>ZZZ</p> <p>PCB HH5A4 LA-M211P LS-M211P 1A DAZ1A@ DAZ3TY00101</p>
	<p>ZZZ</p> <p>PCB 3TY LA-M211P REV1 MB 1 PCB10@ DA8001SW010</p>	<p>ZZZ</p> <p>PCB 3TY LA-M211P REV1A MB 1A PCB1A@ DA8001SW01A</p>

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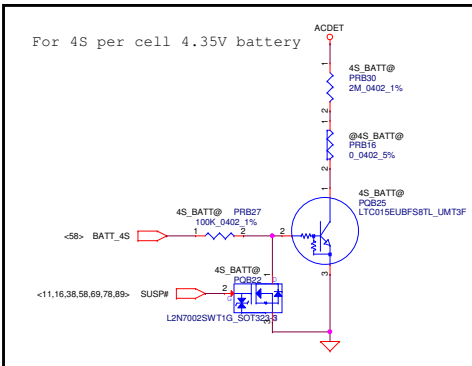
2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

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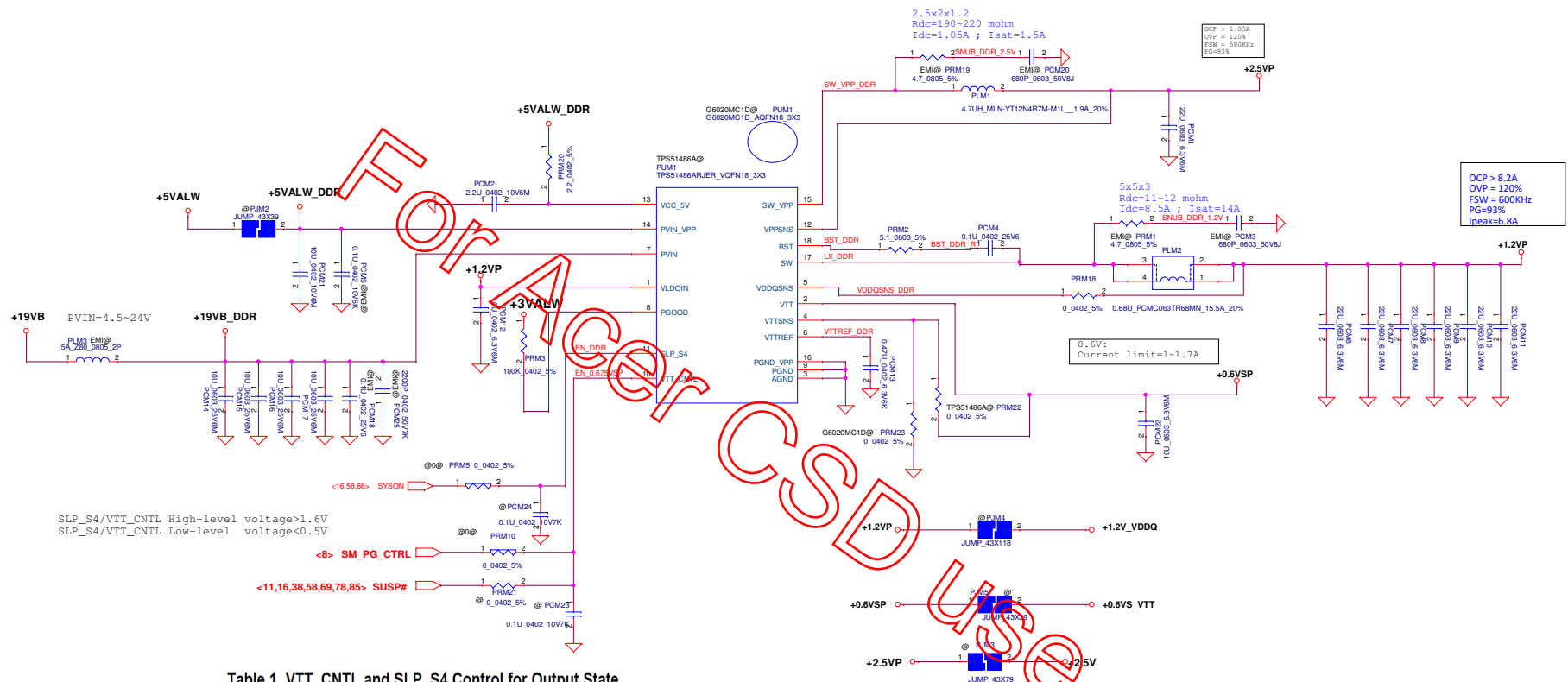
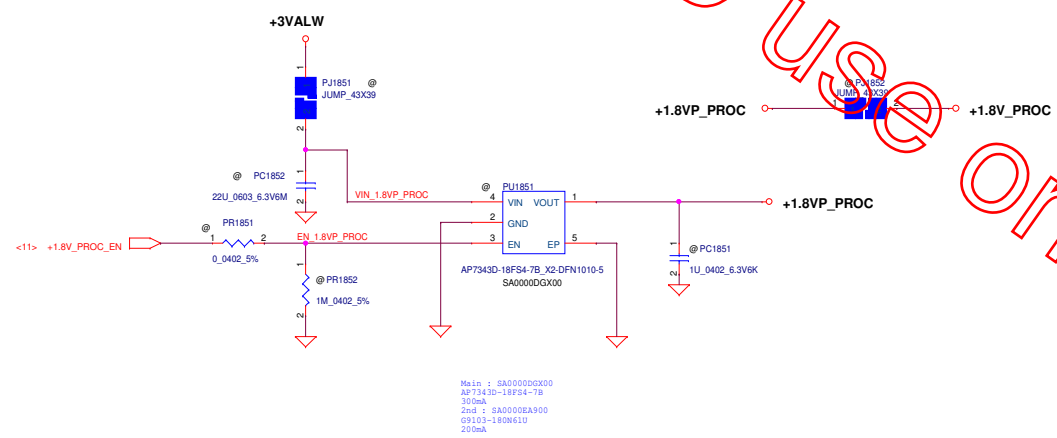
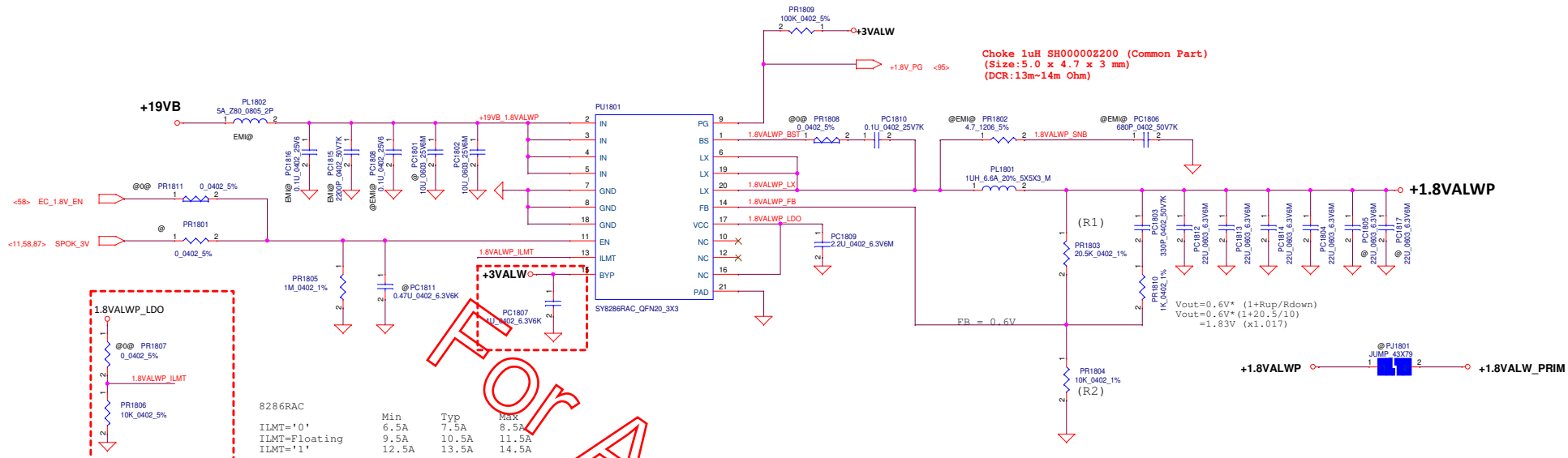


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)



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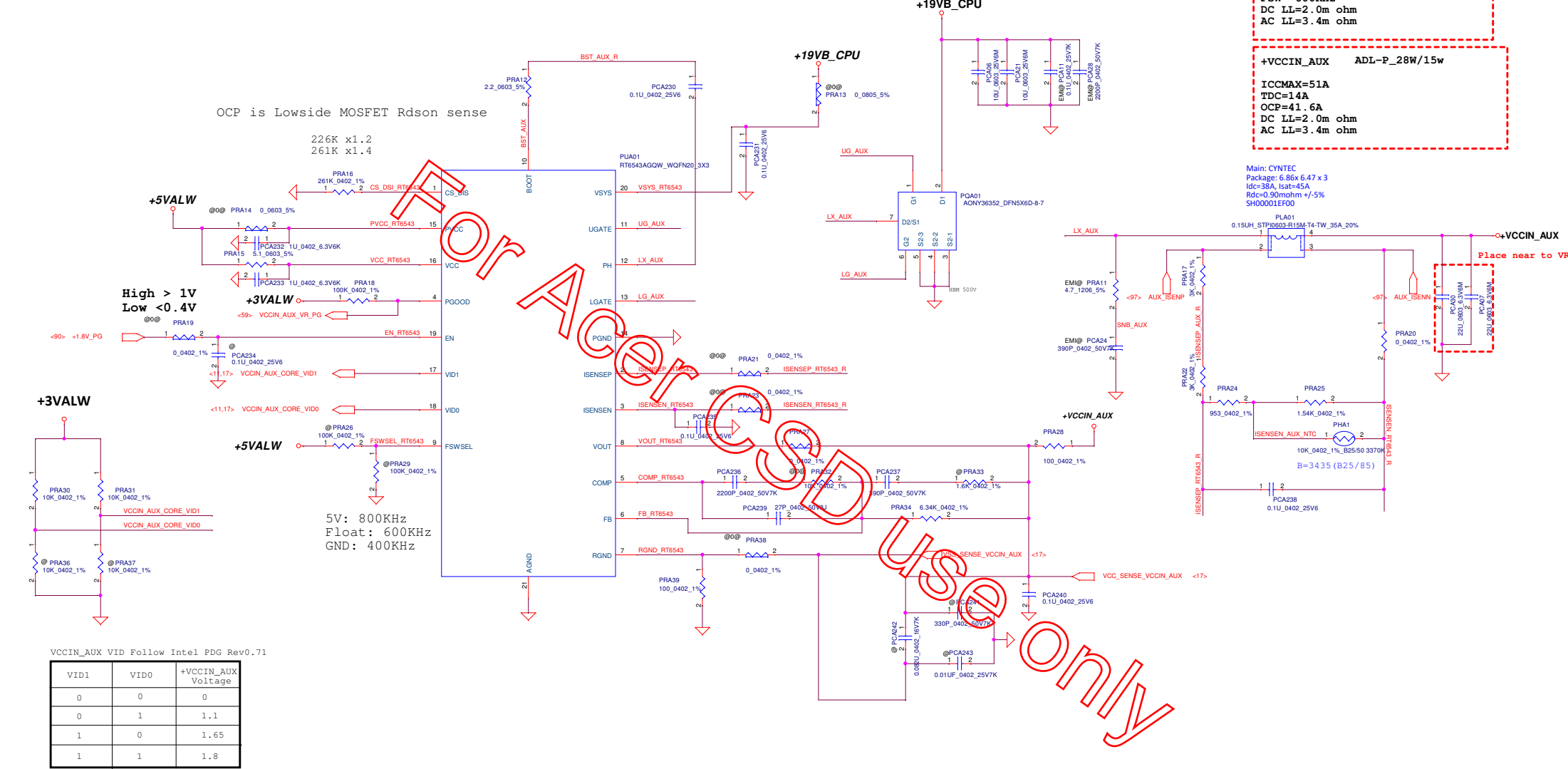
Main Func = +VCCIN_AUX

Module model information
RT6543A_V1A.mdd for IC portion
RT6543A_V1B.mdd for SW portion

+VCCIN_AUX ADL-P_45W
Vout 1.8V
IPL2 (TDC) = 17A
Peak Current = 34.2A (ICCMAX)
OCP: 51A
OVP: VID+0.36V (max 2V)
FSW= 600KHz
DC LL=2.0m ohm
AC LL=3.4m ohm

+VCCIN_AUX ADL-P_28W/15w
ICCMAX=51A
TDC=14A
OCP=41.6A
DC LL=2.0m ohm
AC LL=3.4m ohm

Main: CYNTEC
Package: 6.8x6.47 x 3
Idc=38A, Isat=45A
Rdc=0.90mohm +/-5%
SH00001EF00

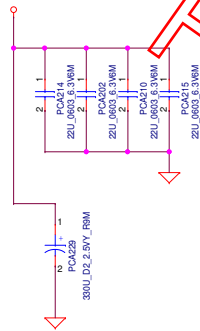


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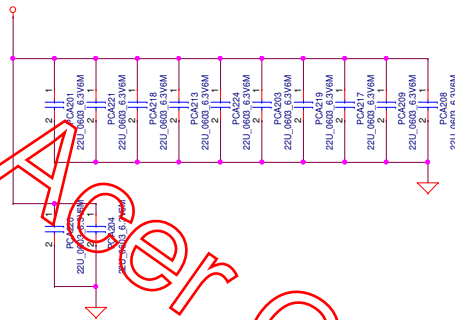
+VCCIN_AUX Output CAP :

330uF_2.5V*1
22uF_0603*18

CPU Primary Side
+VCCIN_AUX



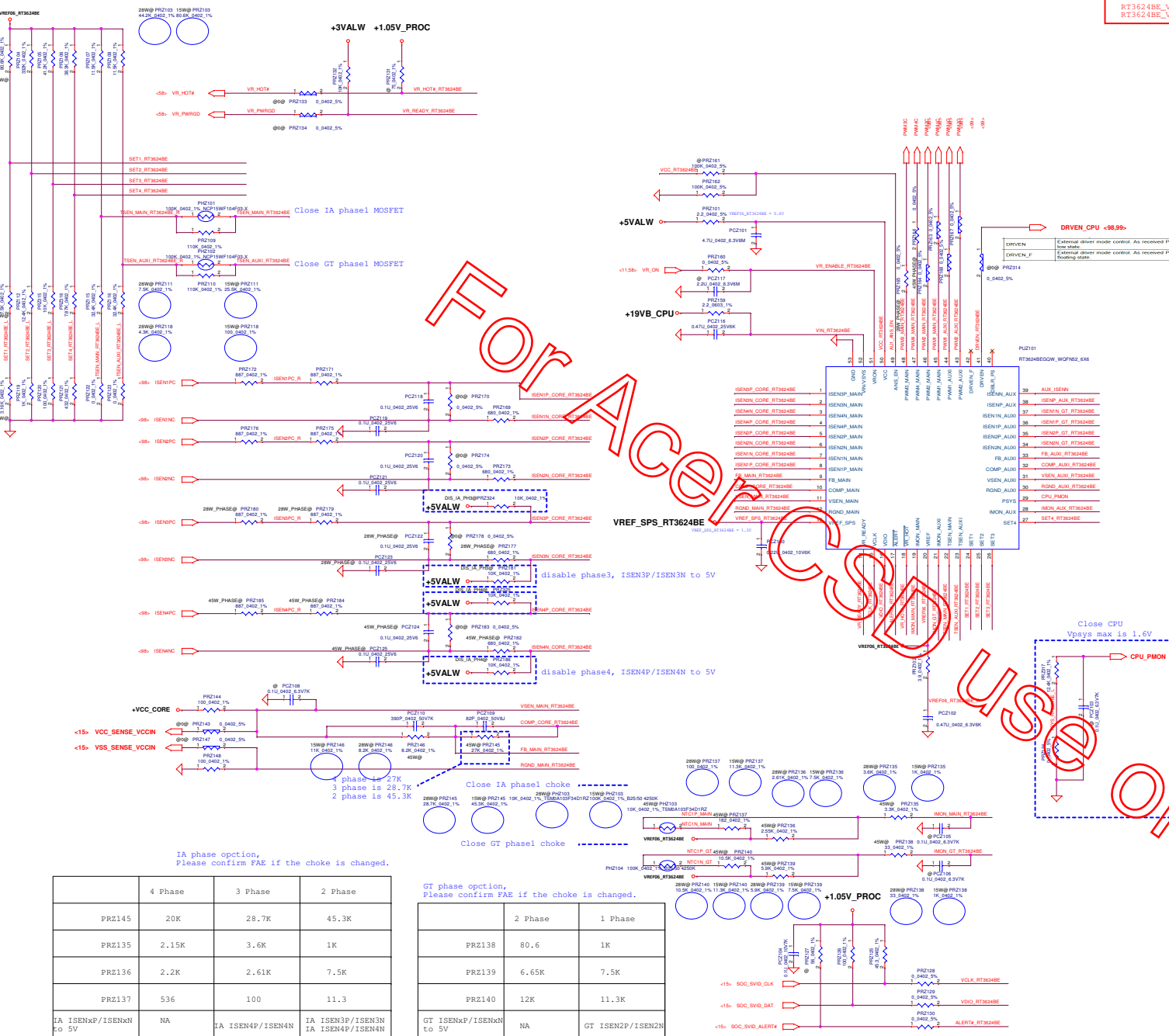
CPU Secondary side
+VCCIN_AUX



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Issued Date	2020/02/27	Deciphered Date	2021/12/31	Title PWR VCCIN AUX DECOUPLING	
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Main Func = CPU (IA/GT)

Module model information
RT3624BE_V1A.mdd IC
RT3624BE_V1B.mdd SW



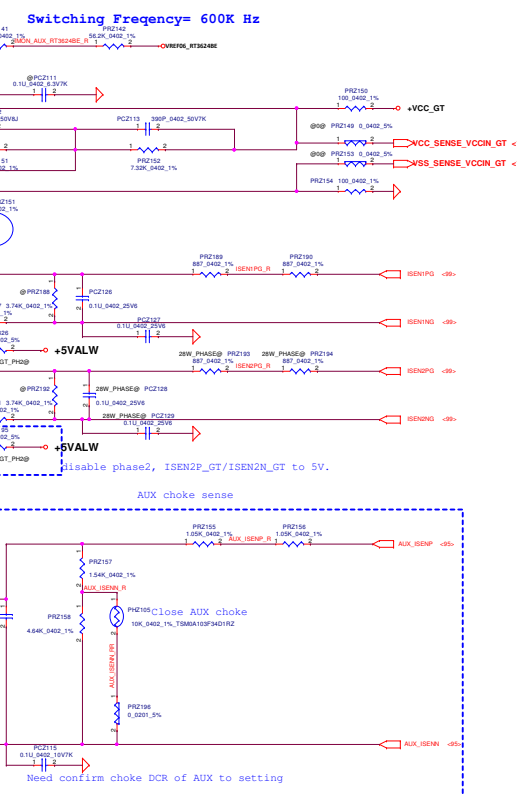
IA phase option,
Please confirm FAE if the choke is changed.

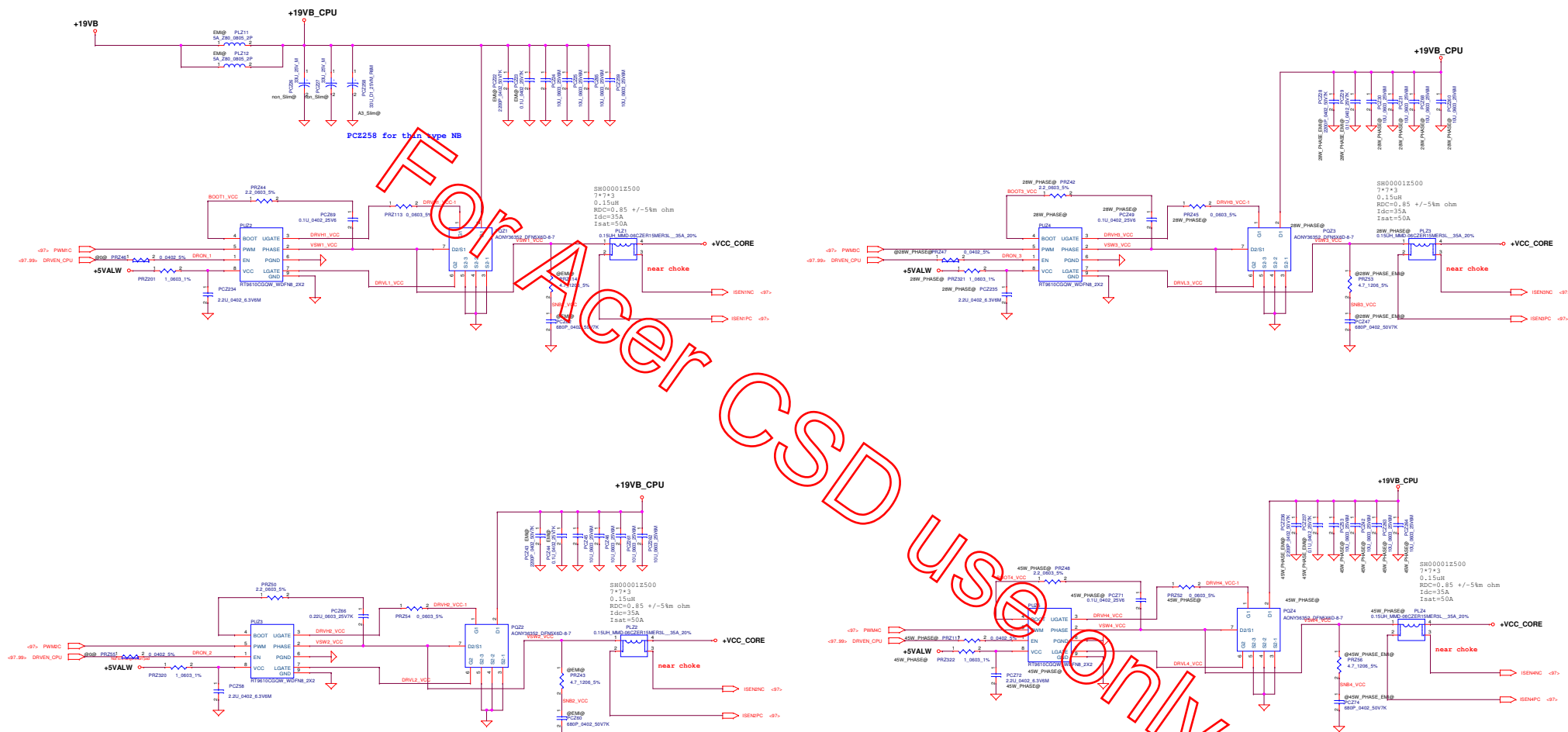
	4 Phase	3 Phase	2 Phase
PRZ145	20K	28.7K	45.3K
PRZ135	2.15K	3.6K	1K
PRZ136	2.2K	2.61K	7.5K
PRZ137	536	100	11.3
IA ISENxP/ISENxN to 5V	NA	IA ISEN4P/ISEN4N	IA ISEN3P/ISEN3N IA ISEN4P/ISEN4N

GT phase option,
Please confirm FAE if the choke is changed.

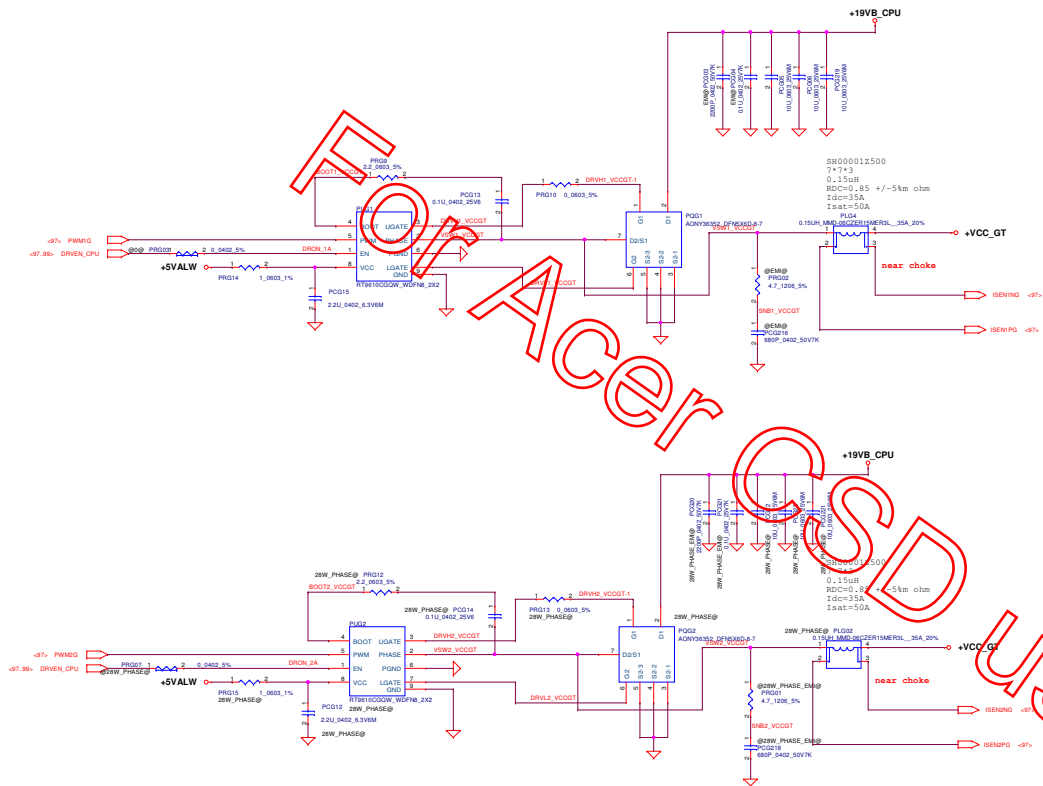
	2 Phase	1 Phase
PRZ138	80.6	1K
PRZ139	6.65K	7.5K
PRZ140	12K	11.3K
GT ISENxP/ISENxN to 5V	NA	GT ISEN2P/ISEN2N

ADI-P_25W	ADI-P_15W	ADI-P_10W
+VCC_CORE ICCMAX=120A TDC=71A OCP=156A DC LL=2.3m ohm AC LL=2.3m ohm	+VCC_CORE ICCMAX=109A TDC=63A OCP=142A DC LL=2.3m ohm AC LL=2.3m ohm	+VCC_CORE ICCMAX=80A TDC=43A OCP=104A DC LL=2.8m ohm AC LL=2.8m ohm
+VCC_GT ICCMAX=55A TDC=30A OCP=65A DC LL=3.2m ohm AC LL=3.2m ohm	+VCC_GT ICCMAX=55A TDC=30A OCP=65A DC LL=3.2m ohm AC LL=3.2m ohm	+VCC_GT ICCMAX=40A TDC=23A OCP=52A DC LL=3.2m ohm AC LL=3.2m ohm
+VCCIN_AUX ICCMAX=34.2A TDC=17A OCP=44.5A DC LL=2.0m ohm AC LL=3.4m ohm	+VCCIN_AUX ICCMAX=32A TDC=14A OCP=41.6A DC LL=2.0m ohm AC LL=3.4m ohm	+VCCIN_AUX ICCMAX=32A TDC=14A OCP=41.6A DC LL=2.0m ohm AC LL=3.4m ohm





Main Func = +VCC_GT



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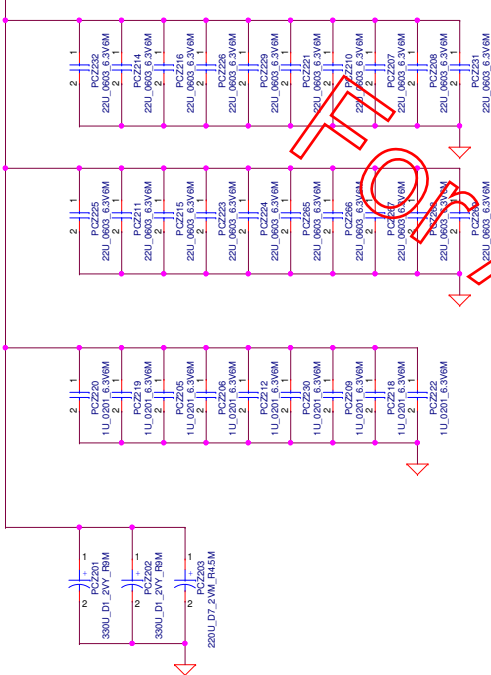
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Main Func = +VCCIN DECOUPLING

+VCC_CORE Output CAP :

330uF*2
220uF*1
22uF_0603*20
1uF_0201*9

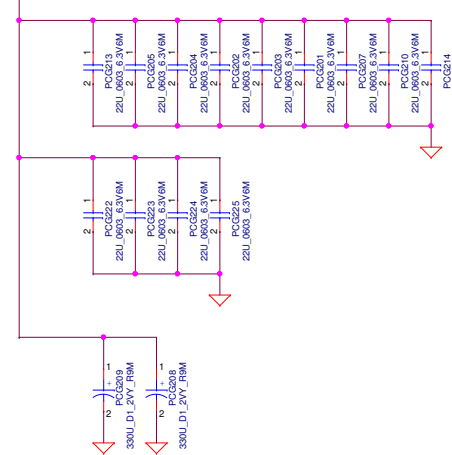
+VCC_CORE



+VCC_GT Output CAP :

330uF*2
22uF_0603*13

+VCC_GT

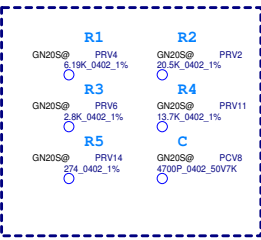


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R1, R2, R3, R4, R5, C are based on VGA type to set.



GB3 -64 =>GN20S
GB3B-64 =>GN18S

Table 2. GB3-64 and GB3B-64 PWM-VID Difference

PWM-VID Specification	GB3-64	GB3B-64	Unit
Vmin	0.3	0.3	V
Vmax	1.3	1.3	V
Vboot	0.75	0.8	V
Voltage Step Vstep	6.25	6.25	mV
Number of Voltage Levels N	160	160	level
PWM Frequency F _{PWM}	675	675	kHz
PWM Minimum Pulse Width T _{MIN}	9.26	9.26	ns
VID Transient Time T	<100	<100	us
Component Value ¹			
R1 [1%]	6.19	6.19	KΩ
R2 [1%]	20.5	20.5	KΩ
R3 [1%]	2.8	4.32	KΩ
R4 [1%]	13.7	16.5	KΩ
R5 [1%]	0.274	0.309	KΩ

GN18-S5	GN20-S5	
GB3B-64	GB3-64	
25		TGP
18.4		TDP
6.5		VRAM TDP
27.7		NVVD TDC
9.6		VRAM TDC
1.6		0.95V TDC
1.7		1.8V TDC
88.5		NVVD Peak
11.7		VRAM Peak
1.9		0.95V Peak
2		1.8V Peak

NVVD OCP :111A

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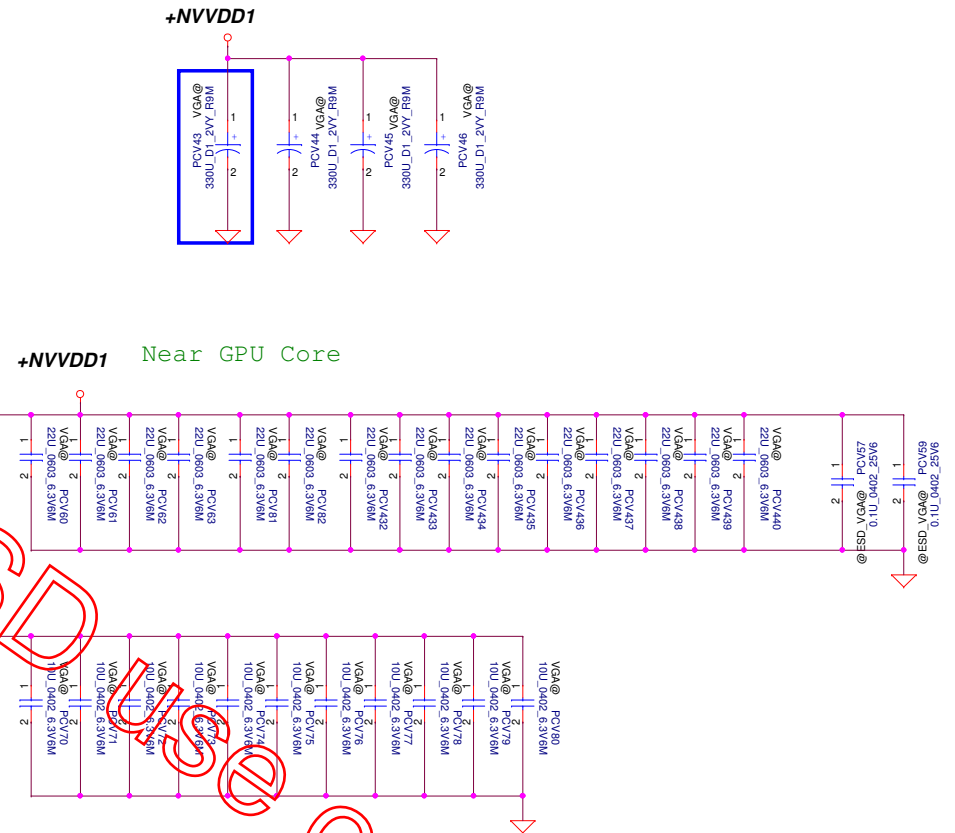
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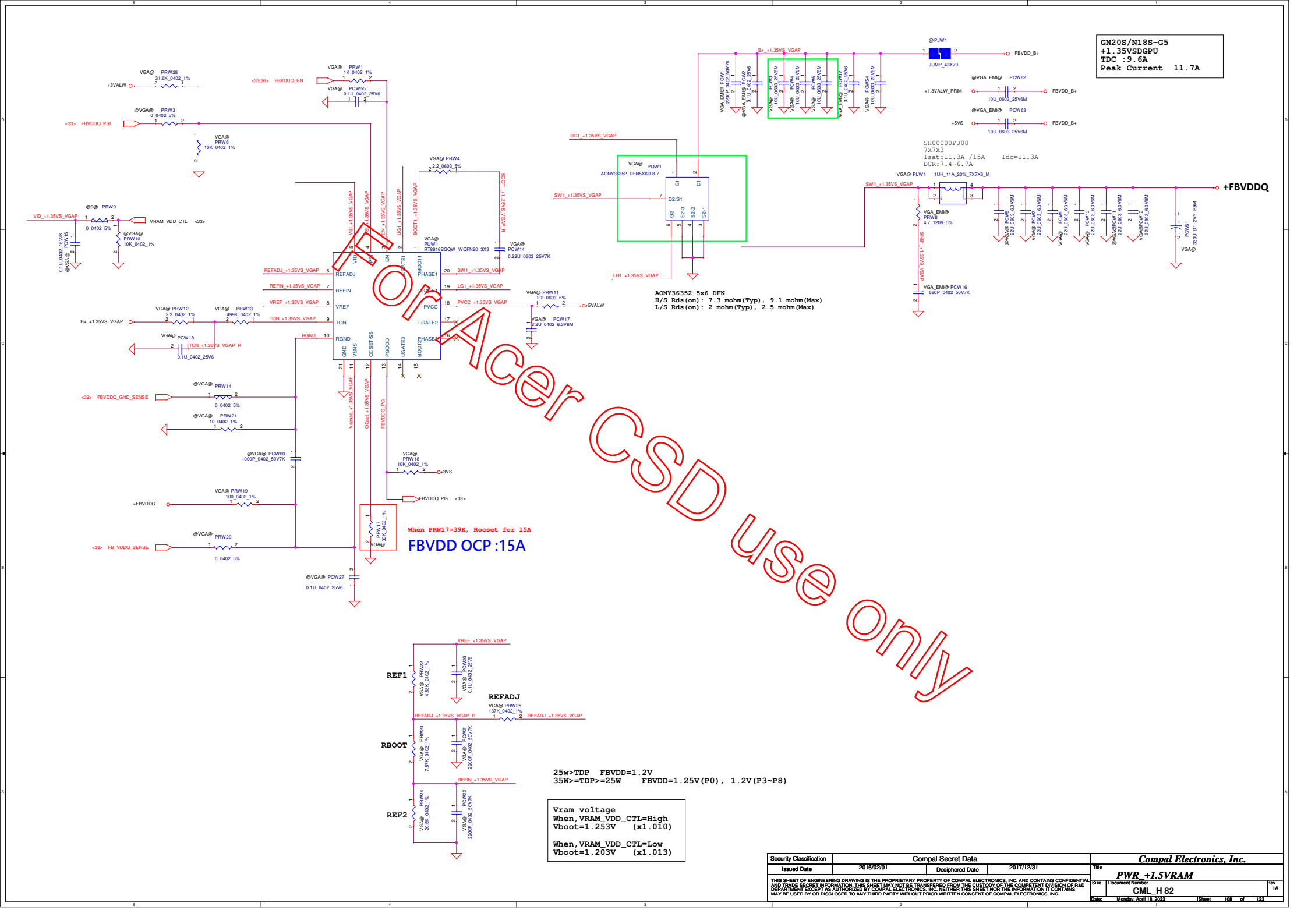
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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
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HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
1	10	9/13	0.2	DMIC Port error	Change DMIC DAT/CLK To GPP_S2/S3
2	33	9/17	0.2	BOM error	Pop RV99 Due to PLTRST_VGA#_1V8 output need pull-up
3	56	9/27	0.2	From Factory request	Remove RA3,RA4
4	52	9/28	0.2	Intel CNVi spec	RW20 Change to 39ohm
5	40	9/30	0.2	ME Connector change	Update HDMI symbol to YUQIU_HD050-F19M0BR-B
6	77	9/30	0.2	Screw hole change	H7 Change to H_3P2
7	56	10/1	0.2	Reserve Mute LED circuit from Codec to KB	Reserve Mute LED circuit
8	58	10/1	0.2	BOM Update	Change R85 to pop
9	6	10/1	0.2	BOM Update	ADD QS CPU PN
10	38	10/5	0.2	Change enable pin to power on TS PWR	Add RVE31 for SUSP# to enable TS PWR
11	29	10/5	0.2	EMI test result update	Add CV322 ,CV323 for EMI Request
12	11	10/5	0.2	Intel Debug port reserve	add test point on GPP_E15/GPP_E16 (intel debug port)
13	8	10/7	0.2	ESD test result update	POP CC5 due to ESD request
14	11	10/7	0.2	BOM Update	UC5 Change to use SA0000BJI00
15		10/7	0.2	BOM Update	Add SAMSUNG 16Gb VRAM part & VRAM Strap pin setting
16		10/7	0.2	BOM reduce	RC256, RO4,RS21,RS25,RS27,RV208 Change to r-short
17		10/7	0.2	BOM reduce	RC1,RC2,RT31,RT33,RA24,RA27,RK5,R72,RC126,RC131,RC200 Change to r-short
18		10/7	0.2	BOM reduce	RO25,RS22,RS23,RS24,RS28,RT12,RT62,RT63,RT64,RT65,RT8,RT9,RT84,RVE3, RVE4 Change to r-short
19		10/7	0.2	BOM reduce	R71,RB11,RB18,RB73,RC186,RC197,RV178,RV211,RV2,RV268,RVE14,RVE15, RVH1,RVH2,RVH3,RVH4,RVH5,RVH6,RVH22 Change to r-short
20	66	10/8	0.2	ESD test result update	DK1 Change to unpop , DK4 change to pop (ESD request)
21	12	10/8	0.2	BOM Update	Pop RC484 for VGA Power up sequence
22	56	10/9	0.2	Vendor Suggest	R1 , R2 Change to 49.9ohm (Vendor request)
23	38	10/18	0.3	Design reserve for QHD panel	Add RVE32 for TS_EN, RVE34 / RVE33 Reserve for QHD PANEL
24	38	10/18	0.3	Design reserve for QHD panel	Reserve PANEL_OD_EN for QHD PANEL
25	56	10/22	0.3	BOM Update	Change codec PN to SA000080Q10
26	69	10/22	0.3	ESD test result update	Pop CS105 from ESD request
27	58	10/22	0.3	DVT BOM Update	Update EC Board ID for A5DVT2@ , A3DVT1@
28	43	11/10	1.0	BOM Update	Change UT14 PN to SA0000DUO10
29	11	11/10	1.0	Reserve for +LCDVDD sequence	Add UVE3/RVE35,RVE36,RVE37 for LCDVDD enable
30	38	11/10	1.0		Change RVE18 to I2C_TS_INT# & Always Pop on (TS Sku & non-TS_Sku)
31	43	11/10	1.0	BBR re-timer leakage issue	RT105 Change to 0 ohm(unpop) , Add DT26 for prevent leakage
32	11	11/10	1.0	EC autoloader power up issue	Add QC2 to EC_VCCST_PG_R prevnet EC autoloader issue
33	38	11/10	1.0		Reserve RVE38,RVE39 for TS_PANEL_OD_EN PU/PD
34		11/14	1.0	BOM reduce	RC143,RC150,RC191, RC34,RK222 , RT108 , RVE22 , RW5,RT1186,RT1187,RT1188, RT4000,RT4001 Change to R-short
35	11	11/14	1.0	EC autoloader power up issue	Reserve QC3 for VR_ON & EC_VCCST_PG_R#
36	43	11/16	1.0	Intel PDG spec update	add RC496 pull-down for PDG 1.5 Version
37	43	11/17	1.0	BBR re-timer leakage issue	Add RT450 pull-up for DG0_RST#
38	43	11/19	1.0	BOM Update	RT1161 Change to 10k ohm
39		11/22	1.0	BOM reduce	RV29 ,RV276,RT209,RV131,RV134,RT300 Change to R-short
40	38	11/22	1.0	ESD test result update	Add CVE23 for ESD request

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Item	Page	Date	Rev.	Reason for change	Modify Item
41	10	11/22	1.0	Net name update	TS_I2C_INT#_GND change to TS_I2C_INT#_R
42	56	11/23	1.0	Reserve for EMI test	RA24,RA27 Change to 0ohm for EMI test
43	58	11/23	1.0	BOM reduce	RB76,RB78 Change to R-short
44		11/29	1.0	BOM update	CS108,CS95,CT536,CT537,CT565 Change to SGA0000F200 , due to SGA00009M00 shortage
45	71	11/29	1.0	BOM update	Add USB Charger X76 PN
46	58	11/29	1.0	BOM update	UK5 change to SA0000BCG50(KB9052Q E)
47	27	11/29	1.0	BOM update	Add GN18-S5 MP PN
48	56	11/29	1.0	BOM update	R1,R2 Change to SD014510A80 (51ohm)
49	16	11/29	1.0	Intel spec update	RC113 Change to 4.7k pull-down
50	16	12/2	1.0	BOM Reduce	RC143,UC5 Change to unpop
51	43	12/2	1.0	BOM update	RT450 Change to 100k pull-up
52	9	12/6	1.0	Reserve for BIOS strap pin	RC481,RC492 Change to pull-down reserve
53	56	12/6	1.0	BOM update	CA31 change to unpop due to PDG no require
54		12/20	1.0	BOM update	Add GN20-S7 /4GB VRAM PN
55		1/14	1.0	BOM update	Add MP CPU PN
56		1/17	1A	PWR update	Combine PWR schematic
57		2/7	1A	BOM update	Update 1A DAZ & Board ID table